

Nirvana 13 UMA Schematics Document

**Sandy Bridge
Intel PCH**

2011-01-18

REV : A00

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DY :None Installed

10mW: External circuit for 10mW solution installed.

BT: Stand alone BT Module.

GSENSOR_ADI: Stuff for ADI G-Sensor.

VCCSA_PWM: Stuff for VCCSA PWM solution.

VCCSA_LDO: Stuff for VCCSA LDO solution.

P2800A1: Stuff for P2800EA1

<Core Design>



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Title

Cover

Size
A3

Document Number

Nirvana 13

Rev

A00

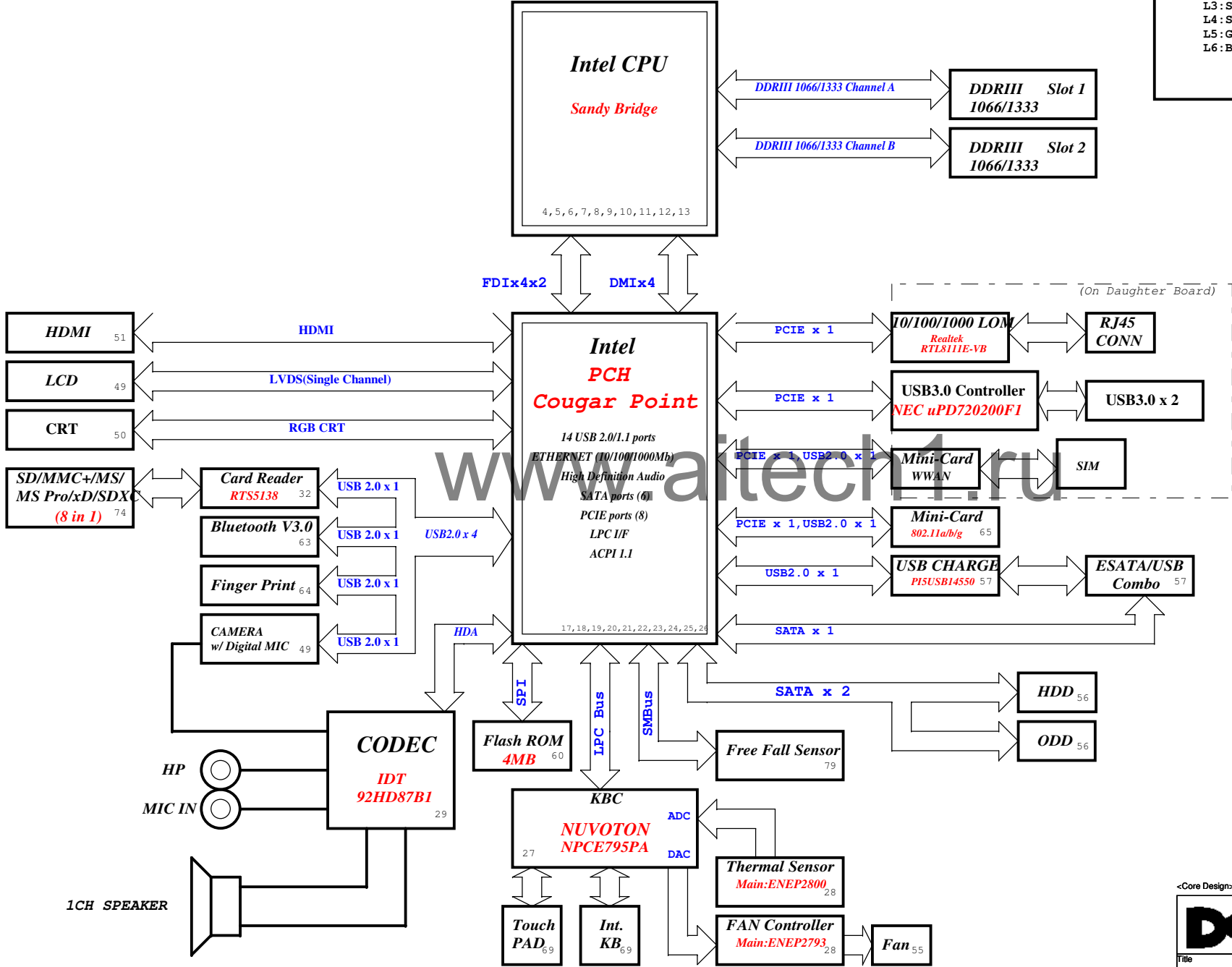
Date: Tuesday, January 18, 2011

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Nirvana 13 UMA Block Diagram
(6 layers)

Project Code: 91.4ID01.001
PCB P/N :10261
Revision :-1

PCB LAYER		CPU DC/DC	
UMA		VT1316+VT1317	42
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Bottom	INPUTS	OUTPUTS	
	5V_S5	VCC_CORE	
	SYSTEM DC/DC		
	VT1316+VT1317		44
	INPUTS	OUTPUTS	
	5V_S5	VCC_GFXCORE	
	SYSTEM DC/DC		
	TPS51461/APL5916		48
	INPUTS	OUTPUTS	
	5V_S5	0D85V_S0	
	SYSTEM DC/DC		
	TPS51216		46
	INPUTS	OUTPUTS	
	DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	
	SYSTEM DC/DC		
	TPS51218		45
	INPUTS	OUTPUTS	
	DCBATOUT	1D05V_VTT	
	TI CHARGER		
	BQ24745		40
	INPUTS	OUTPUTS	
	+DC_IN_S5 +PBATT	DCBATOUT	
	SYSTEM DC/DC		
	TPS51427		41
	INPUTS	OUTPUTS	
	DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5	
	SYSTEM DC/DC		
	TPS51311		47
	INPUTS	OUTPUTS	
	3D3V_S5	1D8V_S0	
	Switches		36
	INPUTS	OUTPUTS	
	1D5V_S3	1D5V_S0	
	5V_S5	5V_S0	
	3D3V_S5	3D3V_S0	



PCH Strapping Huron River Schematic Checklist Rev.1_0

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Enable when Pull-up.
INIT3_3V#	Weak internal pull-up. This signal should not be pulled low. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable Integrated 1.05 V VRMs is enabled when high. This signal should always be pulled high
DF_TVS	DMI and FDI Tx/Rx Termination Voltage Weak internal pull-down. It needs to be connected to PROC_SELECT with a 1K±5% pull-up resistor to PCH VCCPNAND rail and a 4.7K±5% series resistor.
SATA1GP /GPIO19	Boot BIOS Strap bit 0 This signal has a weak internal pull-up. Note: This field determines the destination of accesses to the BIOS memory range. This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC
HDA_SDO	Signal has a weak internal pull-down. Default: the security measures defined in the Flash Descriptor will be in effect. Pull-up: the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing or debug environments ONLY.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. Needs to be pulled High for Huron River platform.
GPIO15	TLS Confidentiality Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: A strong pull-up may be needed for GPIO functionality
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable This signal enables the internal Deep Sleep 1.05 V regulators. This signal must be always pulled-up to VccRTC.
GPIO28	On-Die PLL Voltage Regulator This signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail.

PCIE Routing

LANE1	X
LANE2	LAN (I/O Board)
LANE3	Mini Card2(WWAN)
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	X
1	ESATA / USB COMBO
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Processor Strapping Huron River Schematic Checklist Rev.1_0


Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	0
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded Display Port. 0: Enabled - An external Display Port device is connectd to the Embedded Display Port	1
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.85V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		HURON RIVER ORB	
Device	Ref Des	Address Hex	Bus
EC SMBus 1 Battery Capacity Board			KBC_SDA1/KBC_SCL1 KBC_SDA1/KBC_SCL1
EC SMBus 2 PCH MXM LCD Thermal Sensor			KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
PCH SMBus CK505 Clock Generator SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title Table of Content			
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SSID = CPU

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

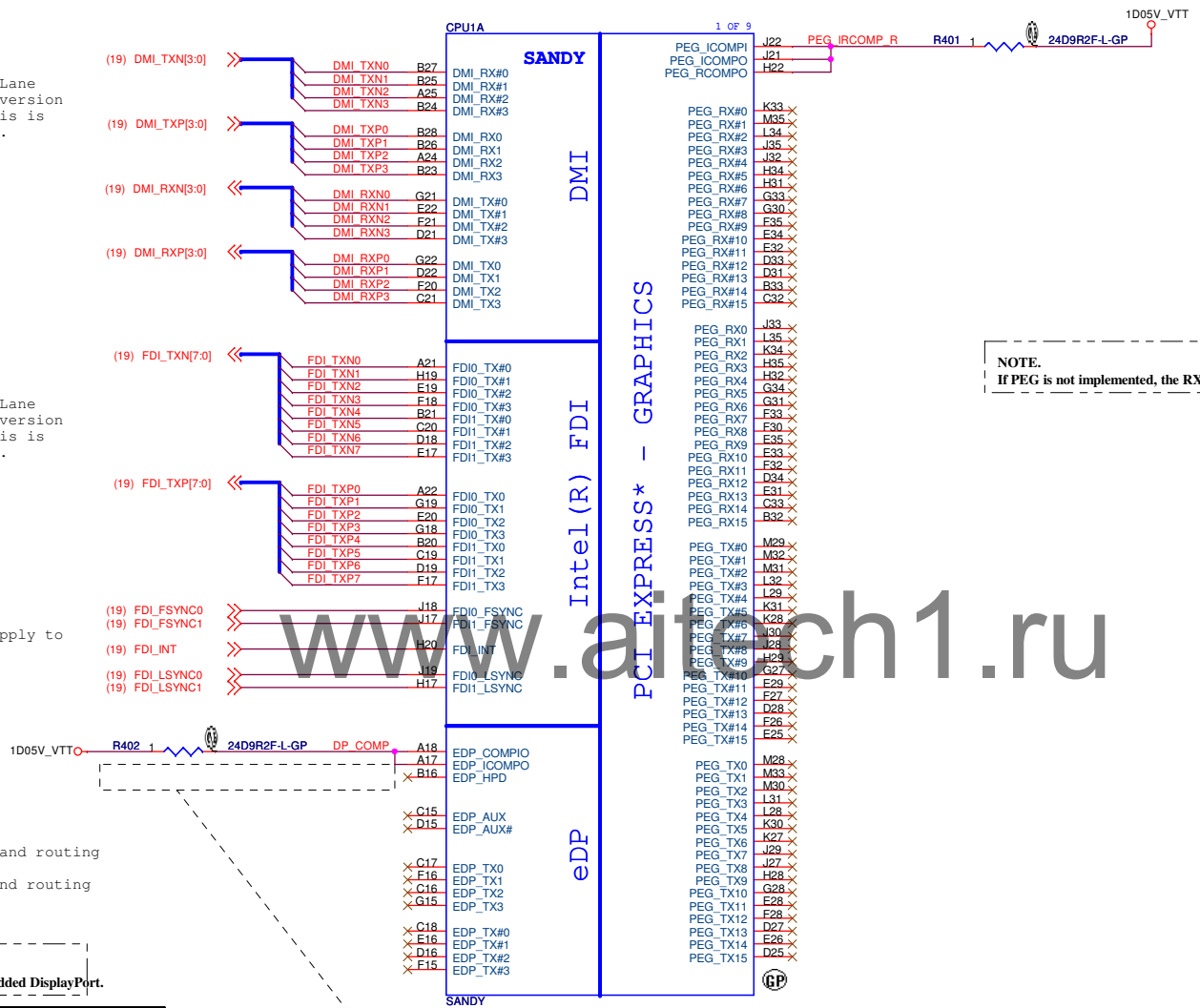
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing
length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing
length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics
function for power saving.

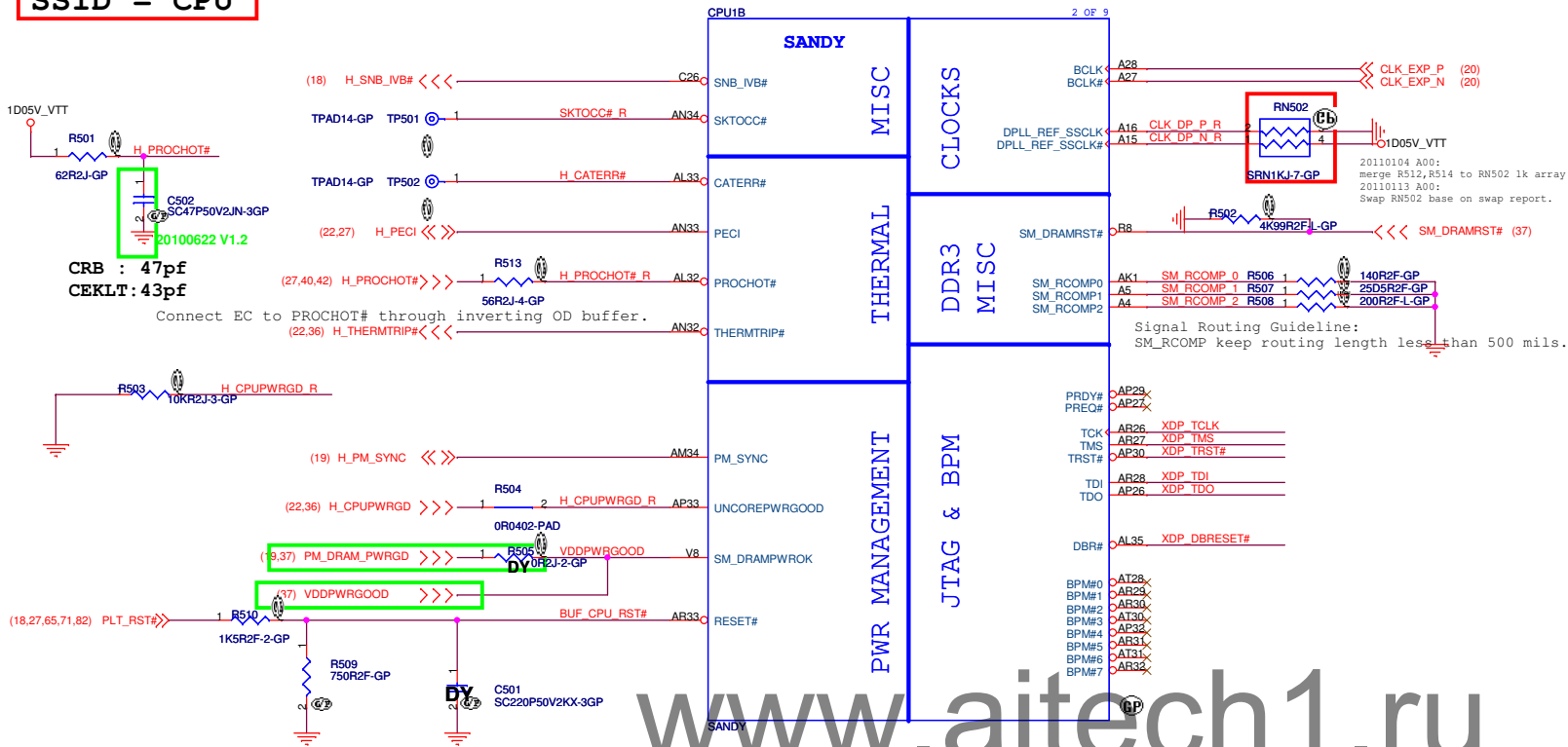
NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up
resistor on the motherboard.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

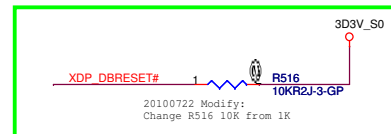
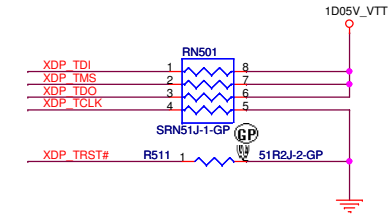


NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

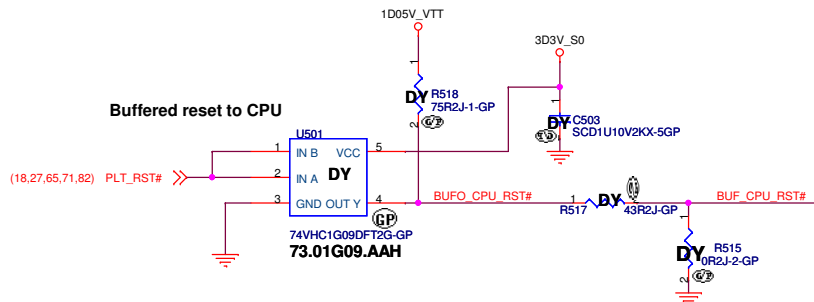
SSID = CPU



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K +/- 5% resistor power (~15 mW) may be
wasted.



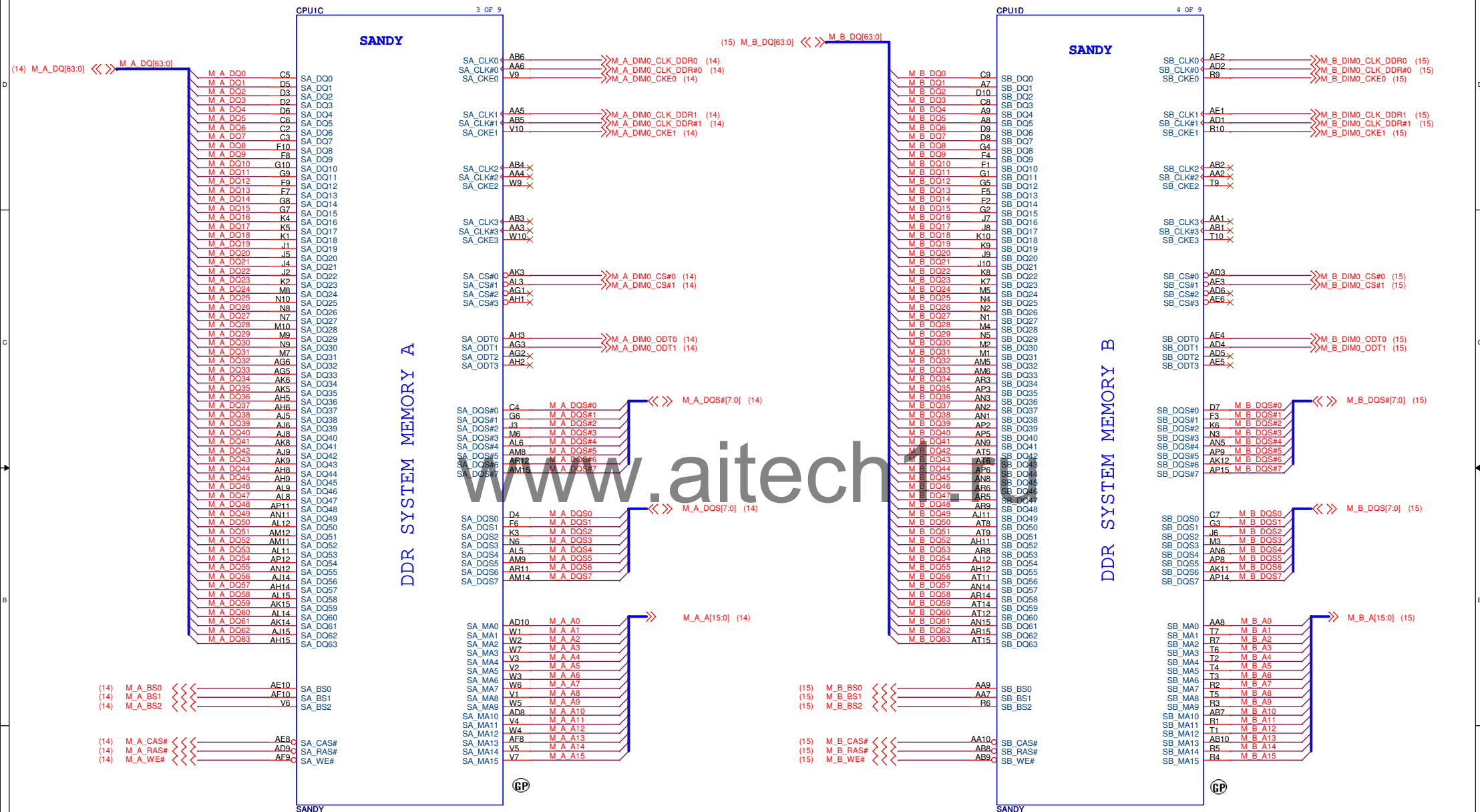
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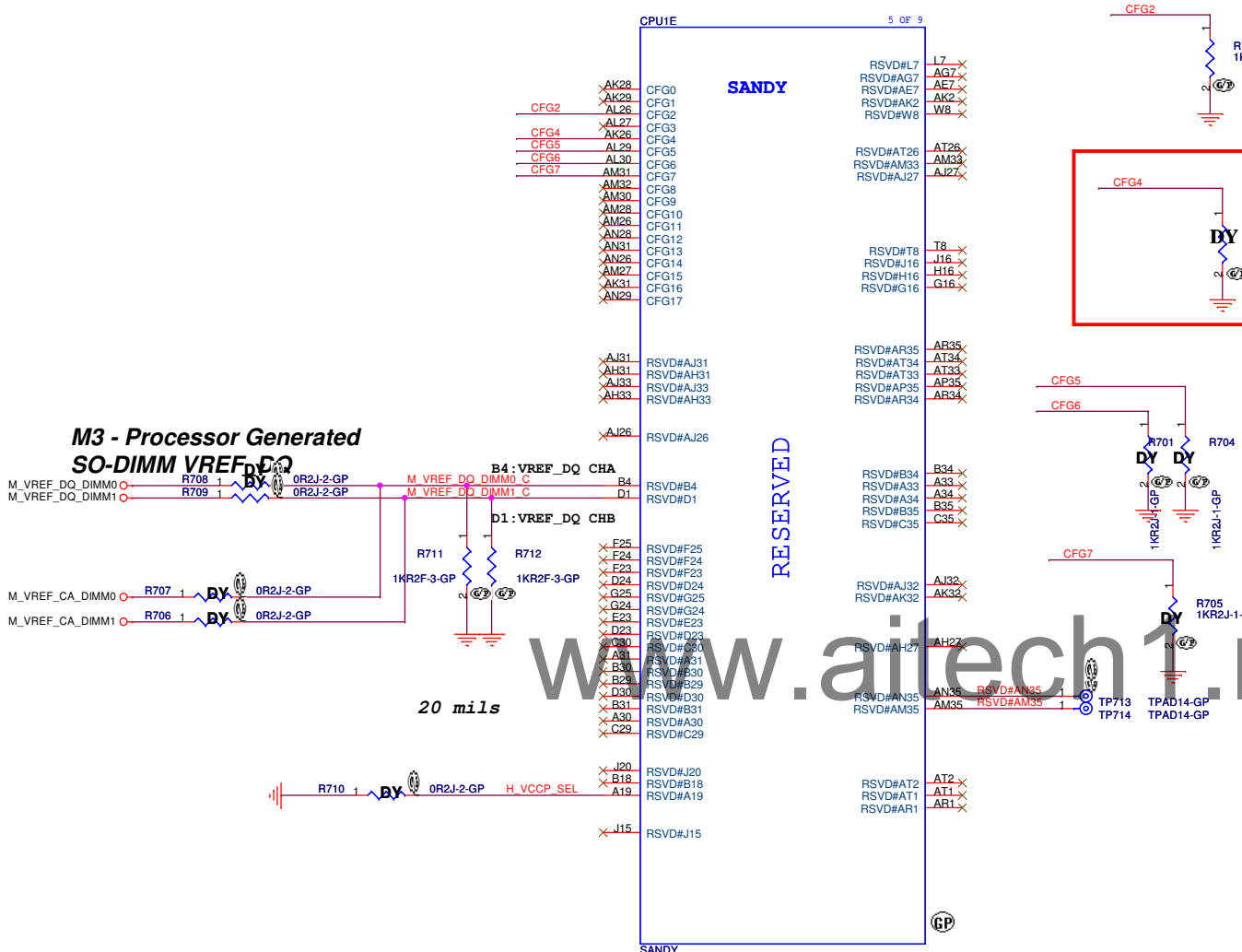
DELL		Wistron Corporation	
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CPU 2/7(THERMAL/CLOCK/PM)			
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SSID = CPU



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SSID = CPU



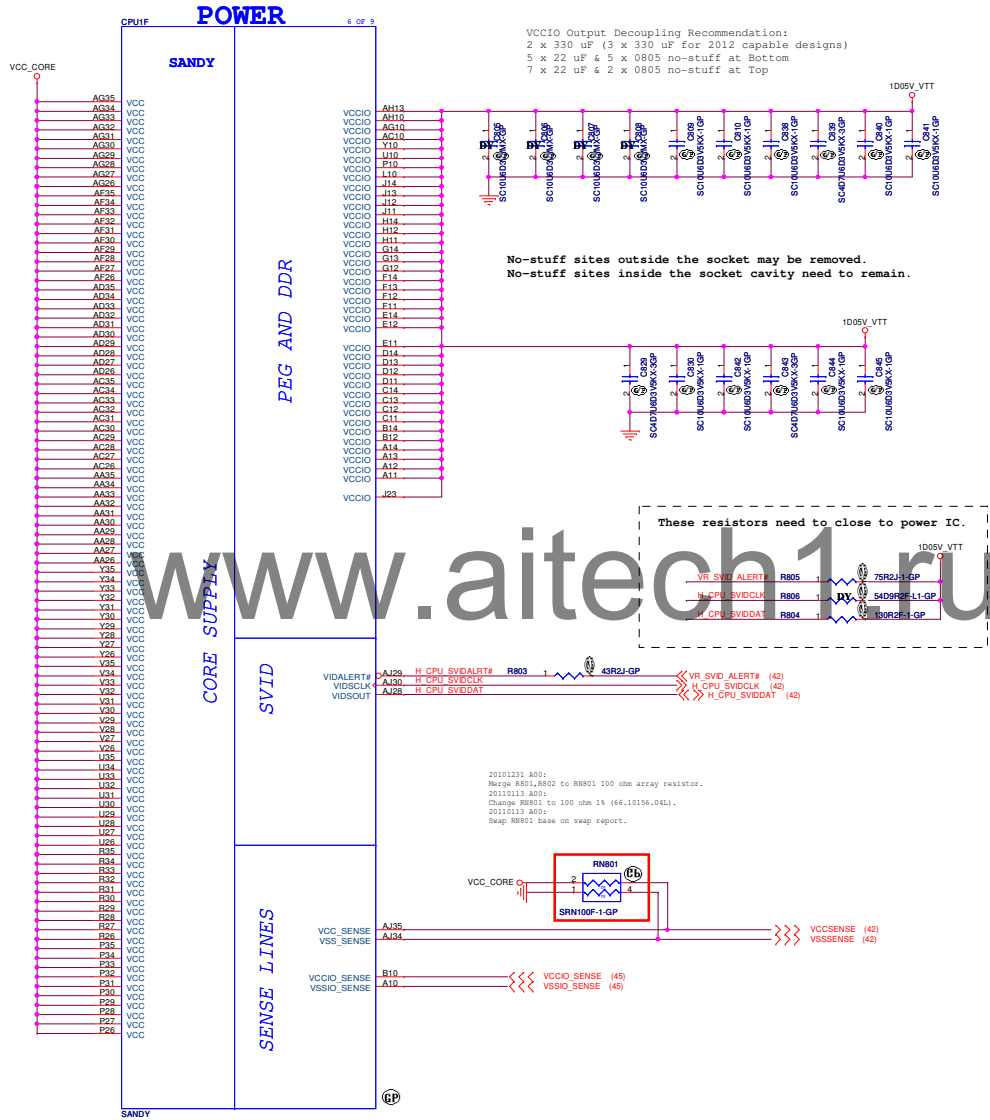
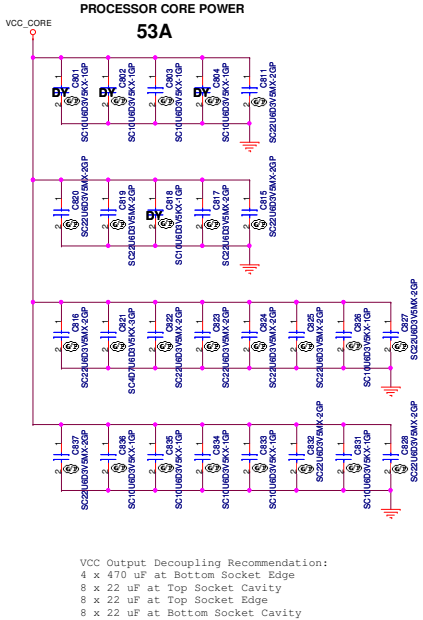
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

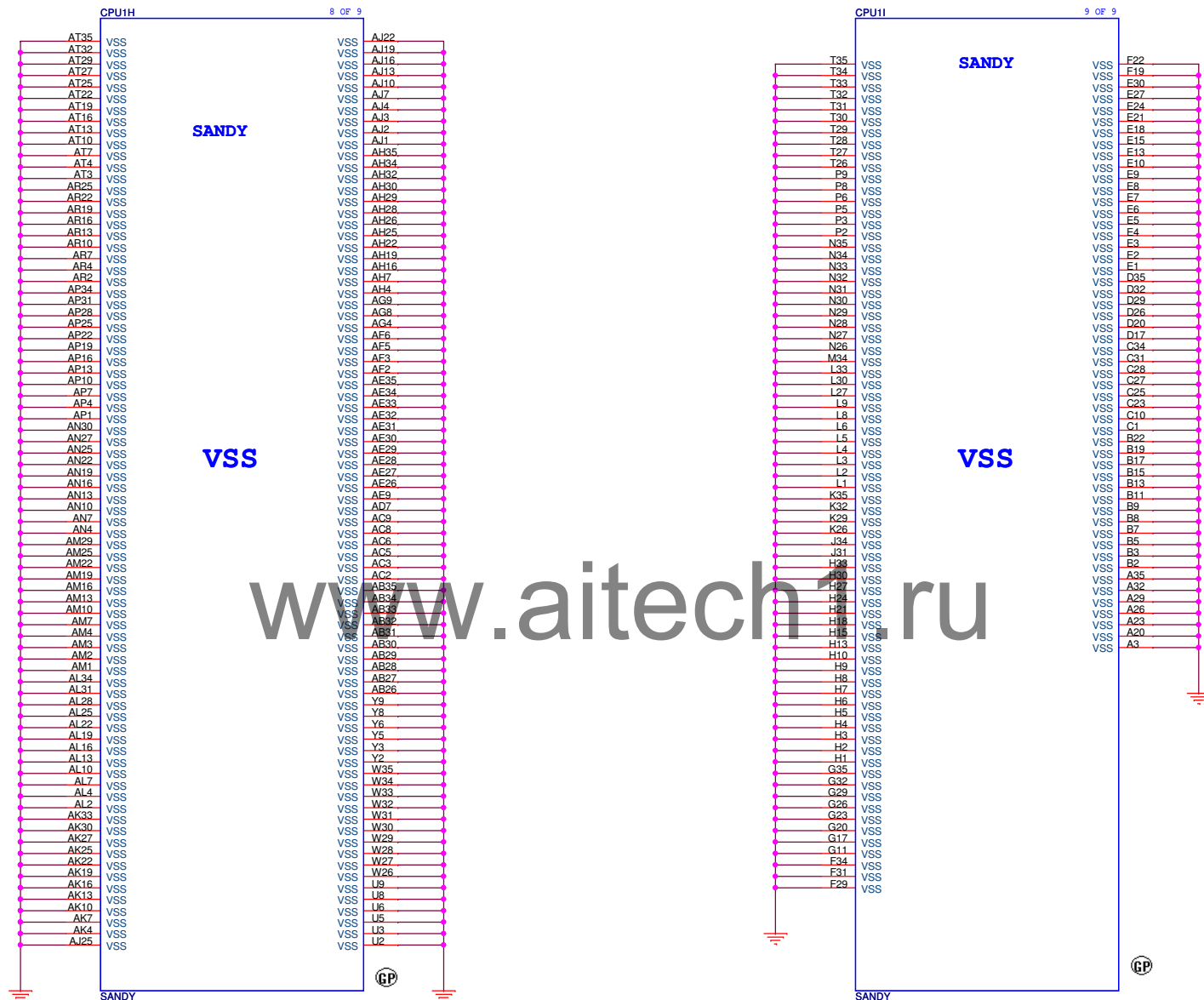
PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A



SSID = CPU




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Remove the XDP connector for space saving 6/28

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Title

Size

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Document Number

Nirvana 13

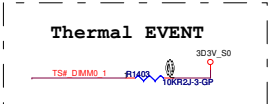
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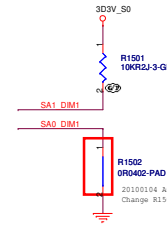
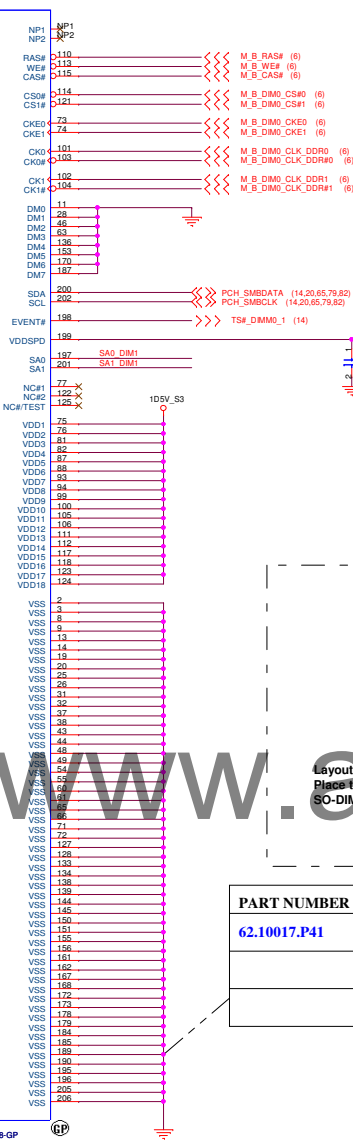
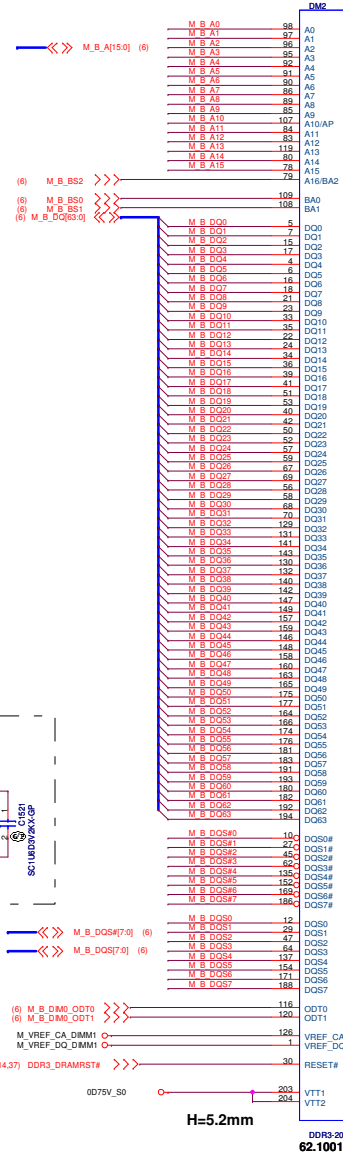
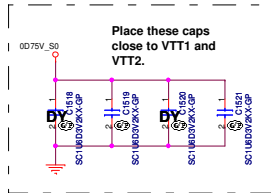
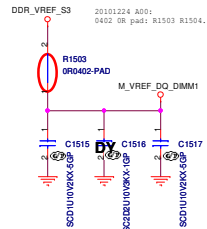
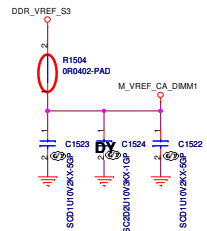
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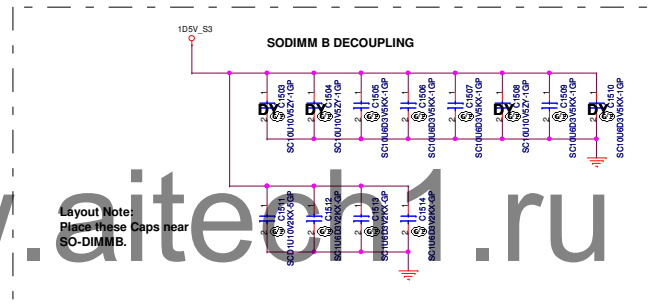
PART NUMBER	Height	TYPE
62.10017.N61	9.2mm	
62.10017.F91		

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA




PART NUMBER	Height	TYPE
62.10017.P41	5.2mm	

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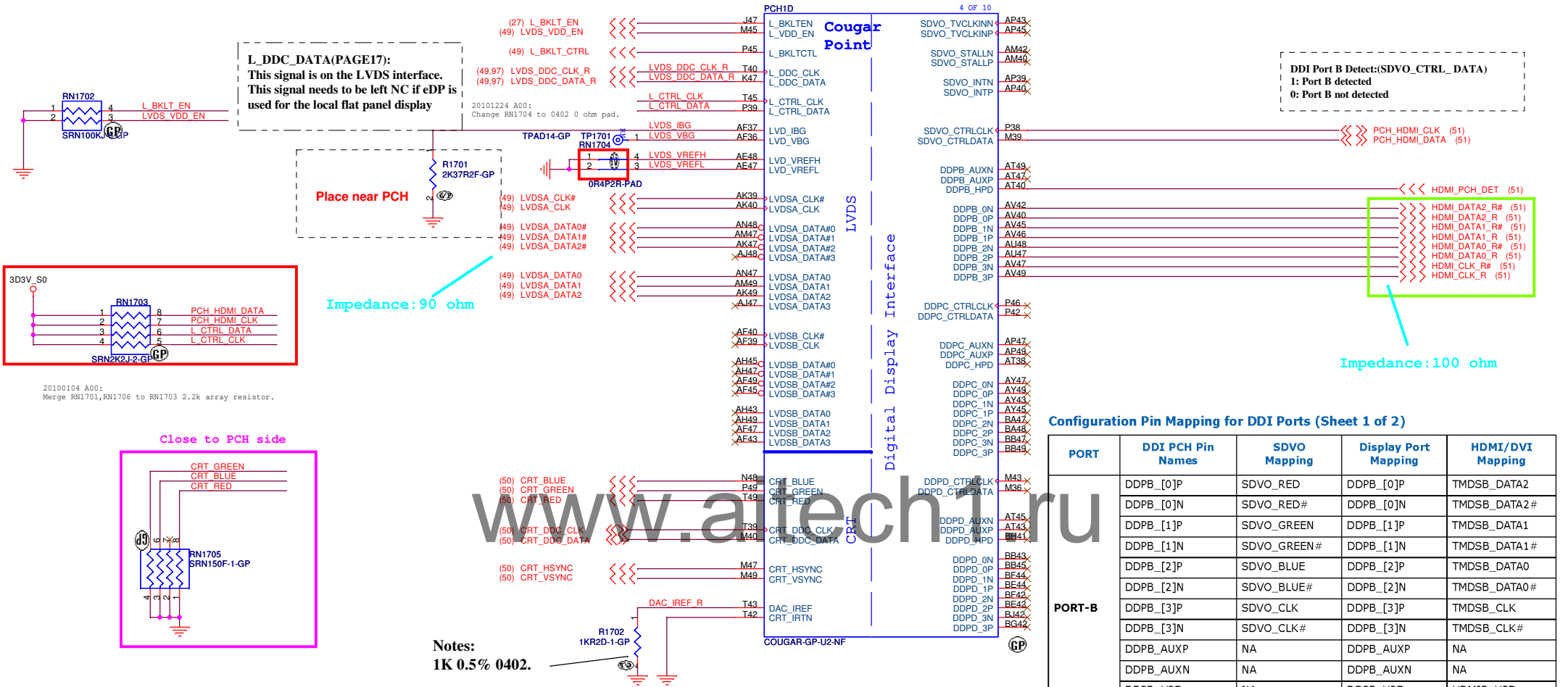
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Date: Wednesday, December 22, 2010

Rev
A00

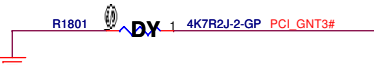
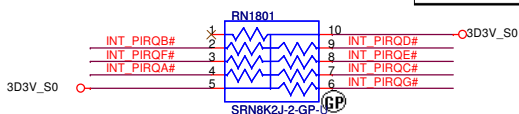
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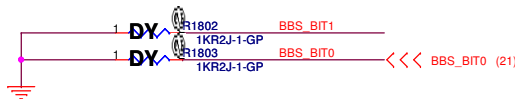
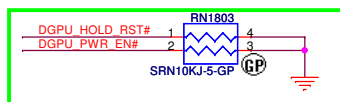
SSID = PCH

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used



Alt6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Alt6 swap override/Top-Block Swap Override enabled High = Default



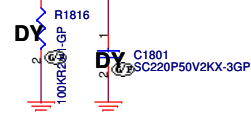
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



20101231 A00:
Merge R1804, R1806 to RN1804 22 ohm array resistor.
20101113 A00:
Swap RN1804 base on swap report.



20101224 A00:
0402 0R pad: R1807.



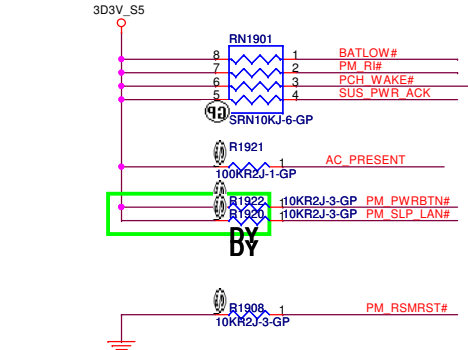
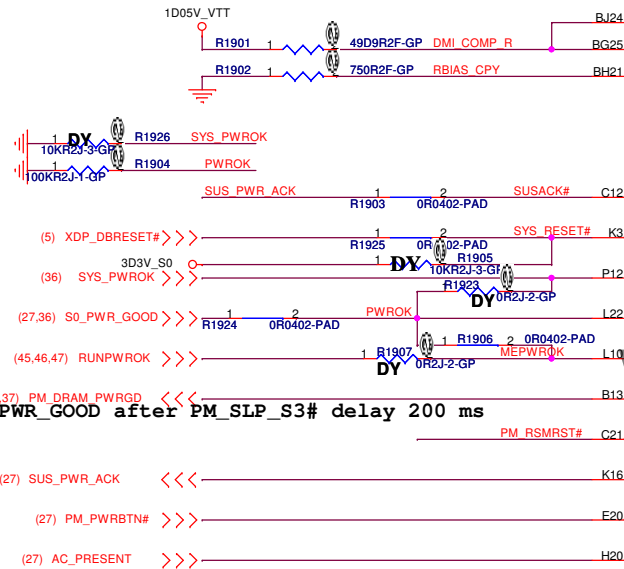
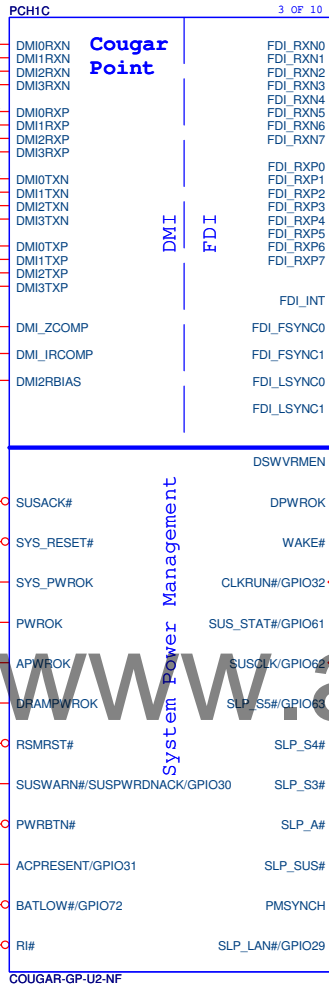
(4) DMI_RXN[3:0]   

(4) DMI_RXP[3:0]   

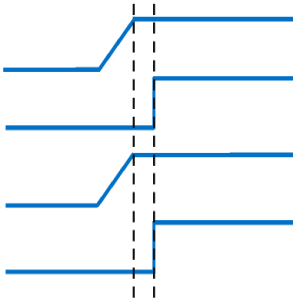
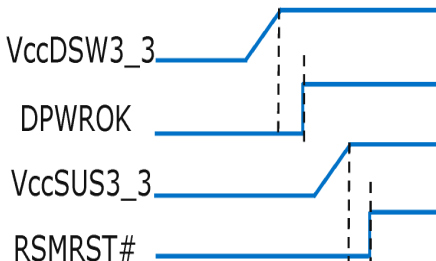
(4) DMI_TXN[3:0]   

(4) DMI_TXP[3:0]   

(4)	DML_RXN0	>>>	
(4)	DML_RXN1	>>>	
(4)	DML_RXN2	>>>	
(4)	DML_RXN3	>>>	
(4)	DML_RXP0	>>>	
(4)	DML_RXP1	>>>	
(4)	DML_RXP2	>>>	
(4)	DML_RXP3	>>>	
(4)	DML_TXN0	<<<	
(4)	DML_TXN1	<<<	
(4)	DML_TXN2	<<<	
(4)	DML_TXN3	<<<	
(4)	DML_TXP0	<<<	
(4)	DML_TXP1	<<<	
(4)	DML_TXP2	<<<	
(4)	DML_TXP3	<<<	



Deep S4/S5 **Not** Supported

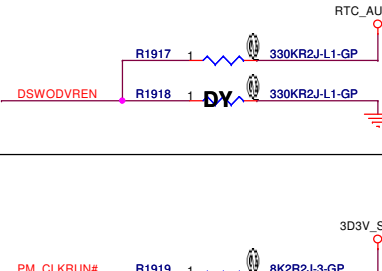


For platforms not supporting Deep S4/S5

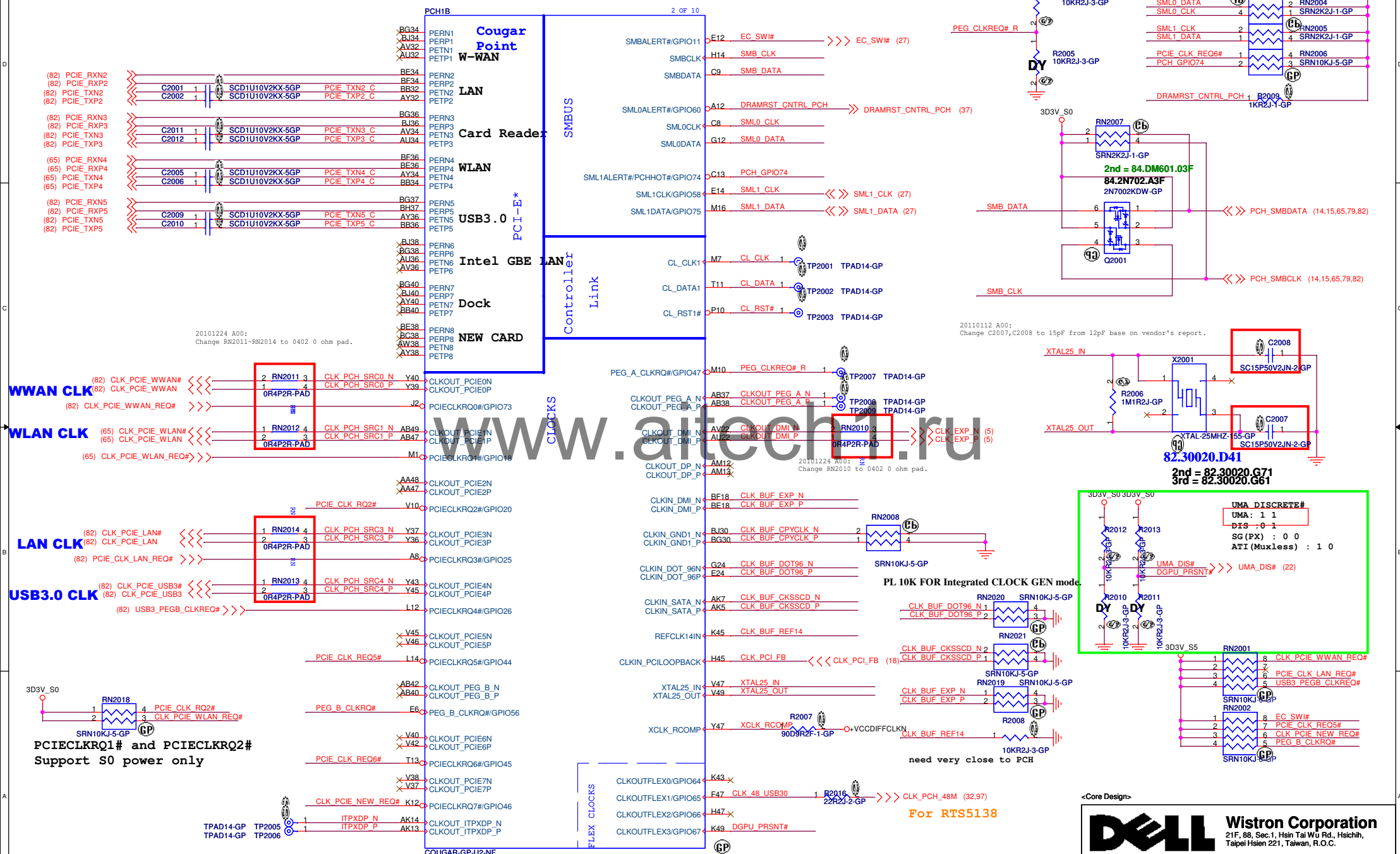
- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)**
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)**
- 3.SLP_SUS# and SUSACK# are left as ‘no connect’**
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30**

DSWODVREN - On Die DSX VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

The diagram shows a circuit for the DSWODVREN signal. A red line labeled DSWODVREN is connected to pin 1 of a relay labeled R1918 (330KR2J-L1-GP). The other side of R1918 is connected to pin 1 of another relay labeled R1917 (330KR2J-L1-GP). The other side of R1917 is connected to the RTC_AUX_S5 pin, which is also connected to ground.

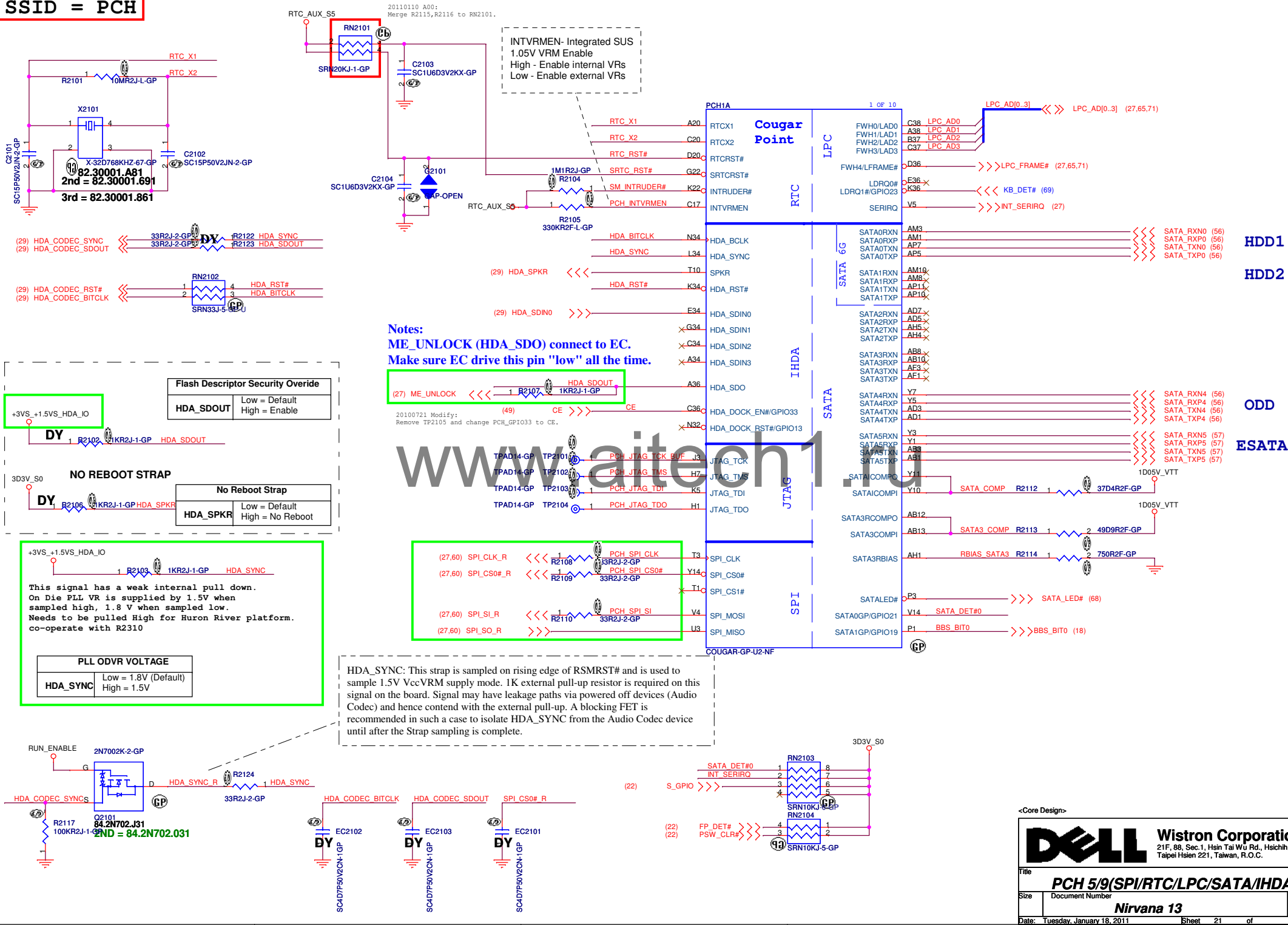


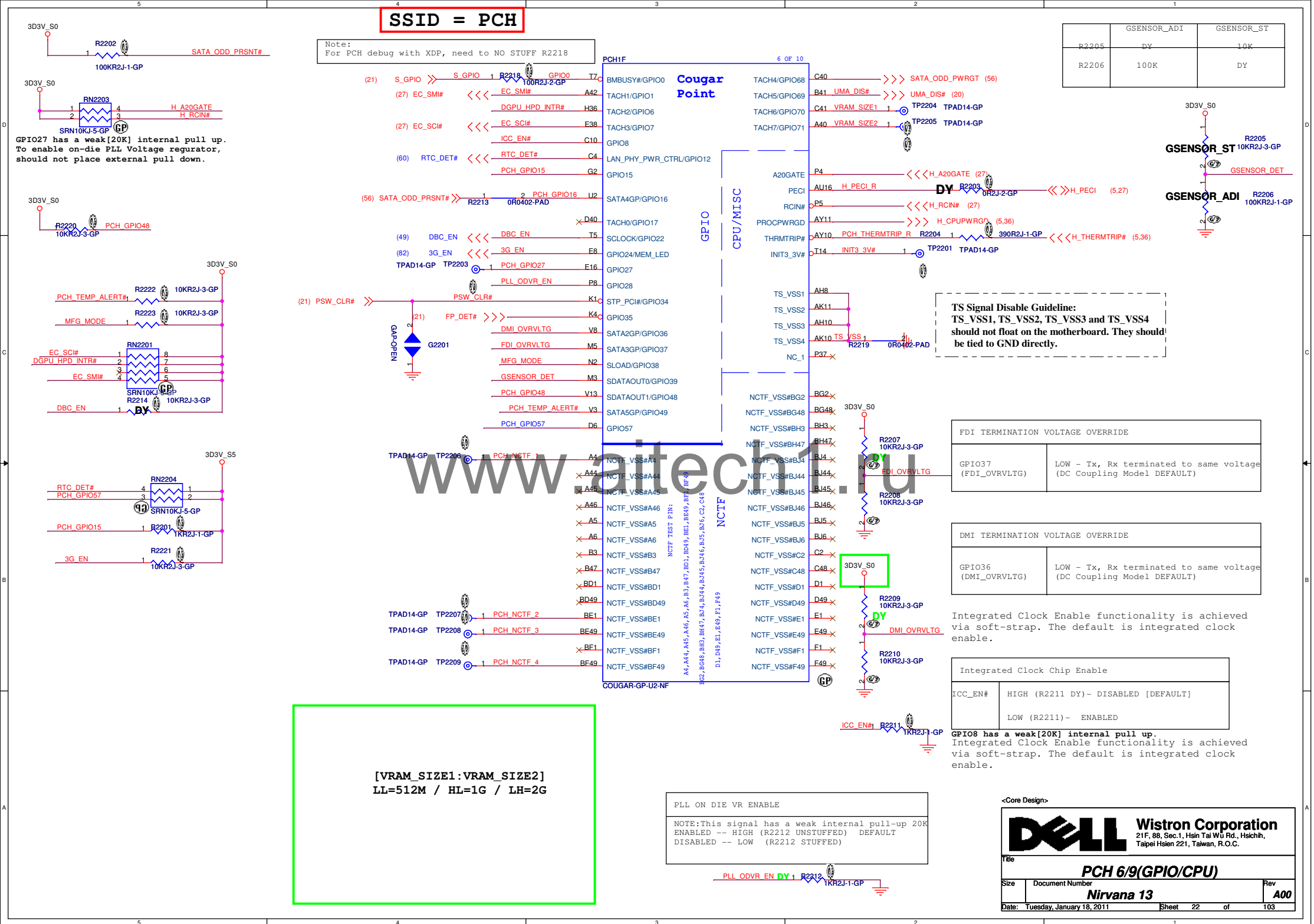
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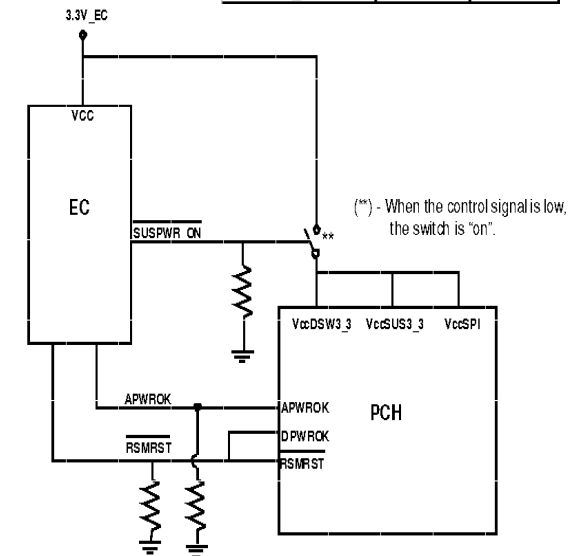
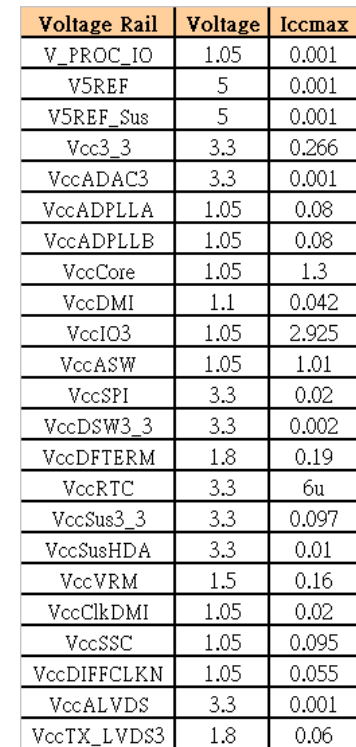
- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

SSID = PCH





6A



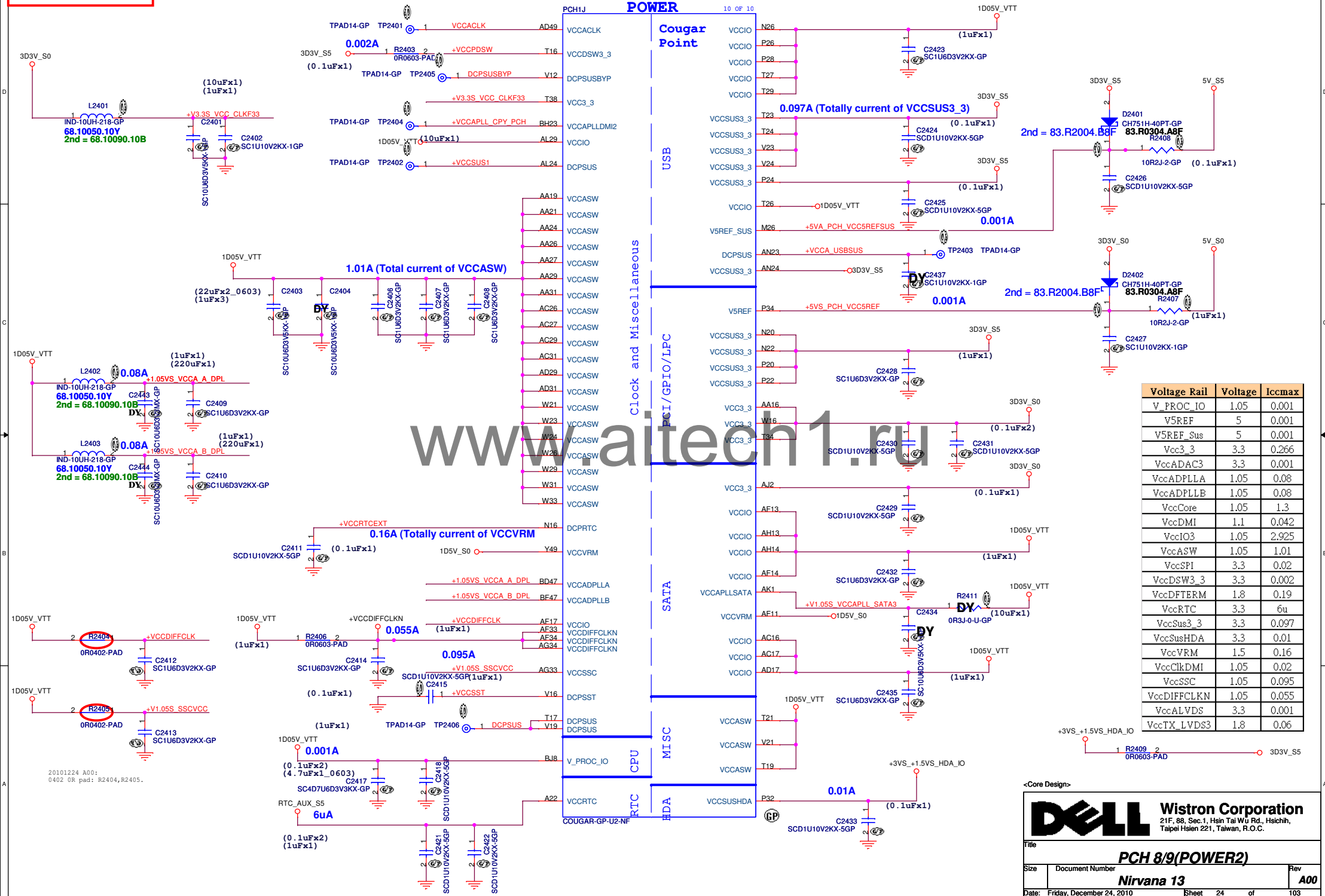
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Title			
PCH 7/9(POWER1)			
Size	Document Number		Rev
	Nirvana 13		A0
Date:	Wednesday, December 29, 2010	Sheet 23 of	103

SSID = PCH

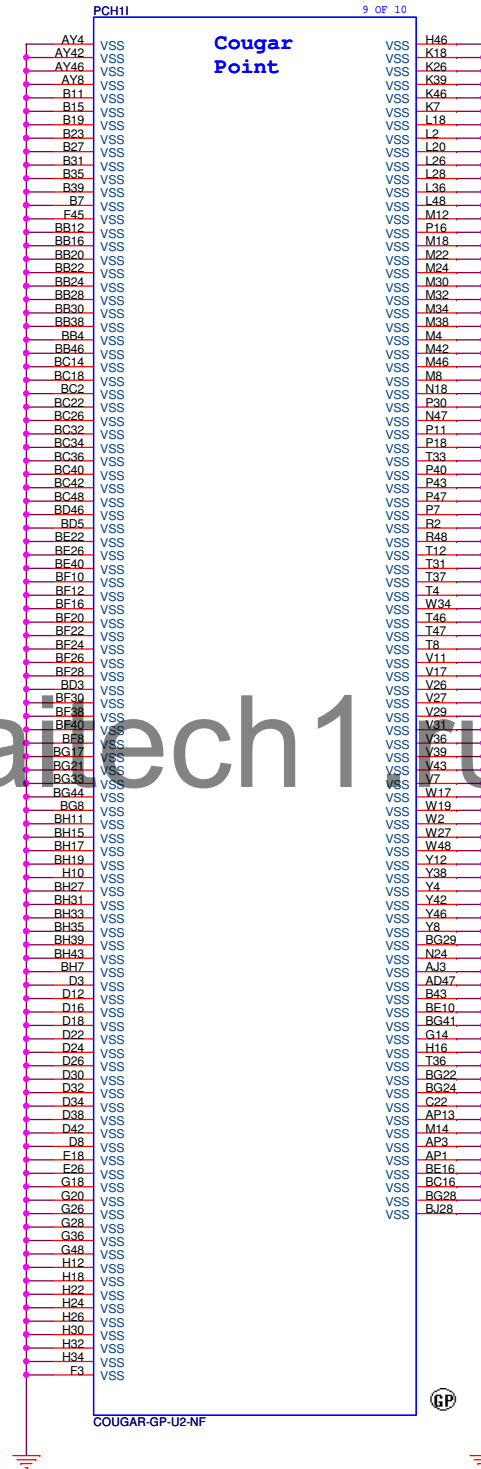
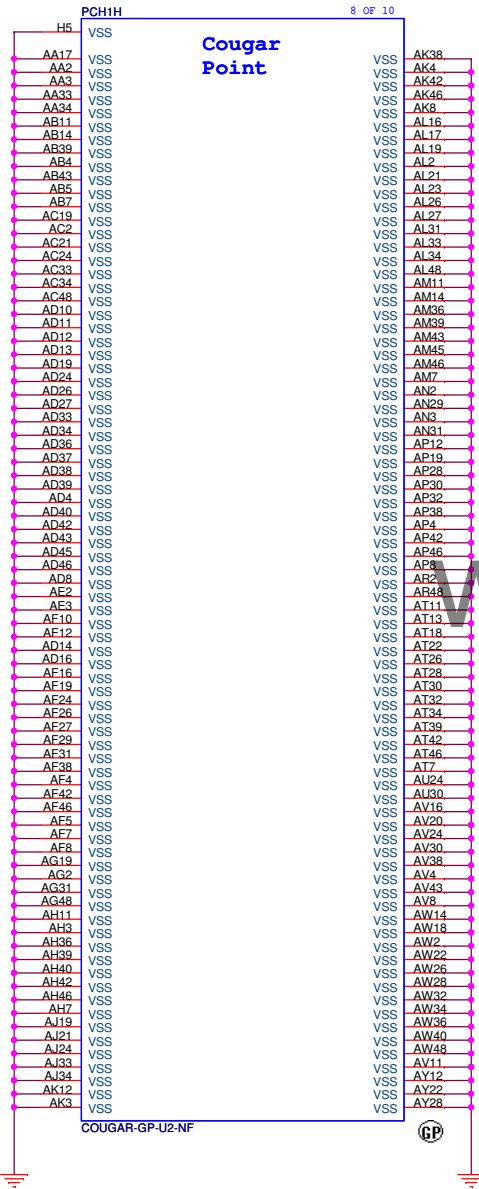


Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLL	1.05	0.08
VccADPLL	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTerm	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

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Title			
		PCH 8/9(POWER2)	
Size	Document Number	Rev	
	Nirvana 13	A00	
Date:	Friday, December 24, 2010	Sheet	24 of 103

SSID = PCH



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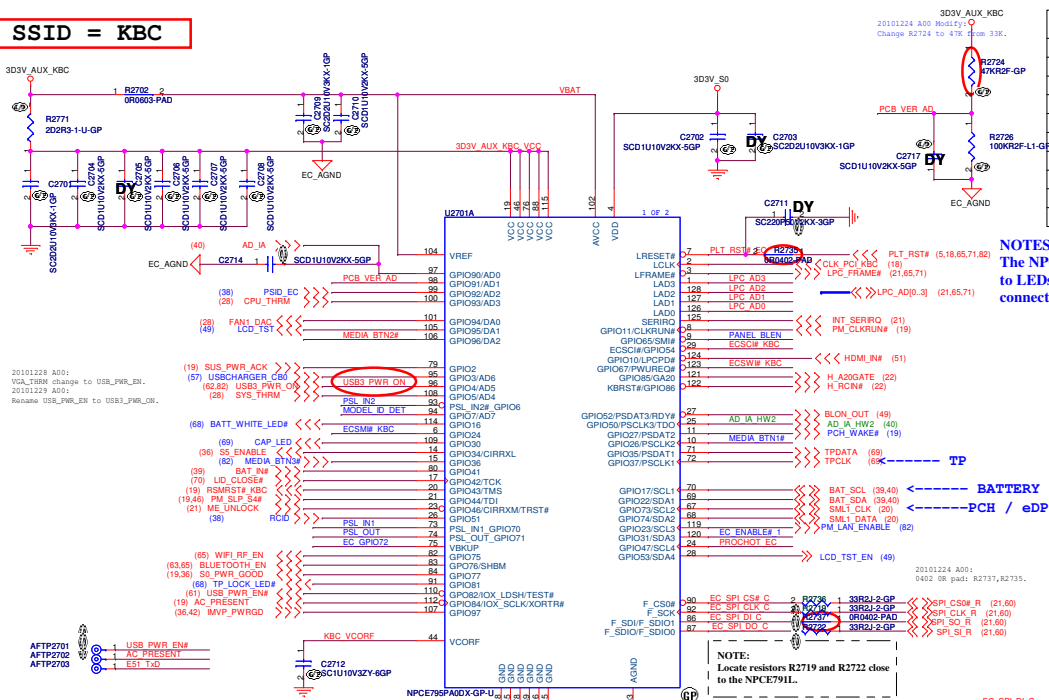
Title

Reserved

Size	Document Number	Rev
A3	Nirvana 13	A00

Date: Wednesday, December 22, 2010	Sheet 26 of 103
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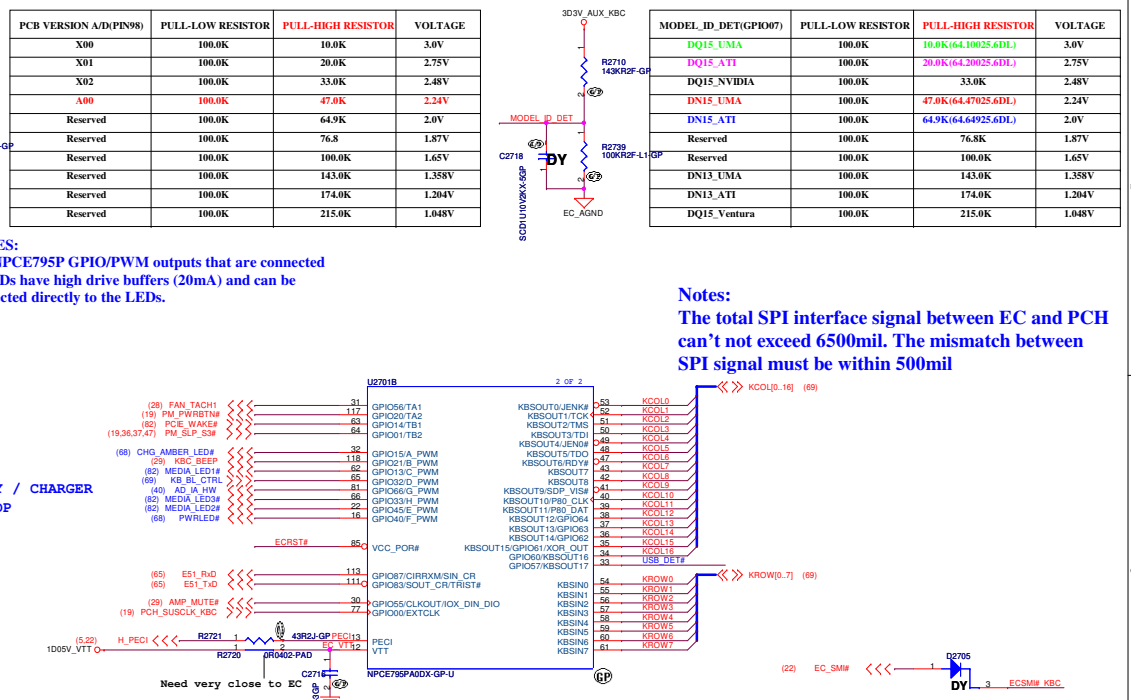
SSID = KBC



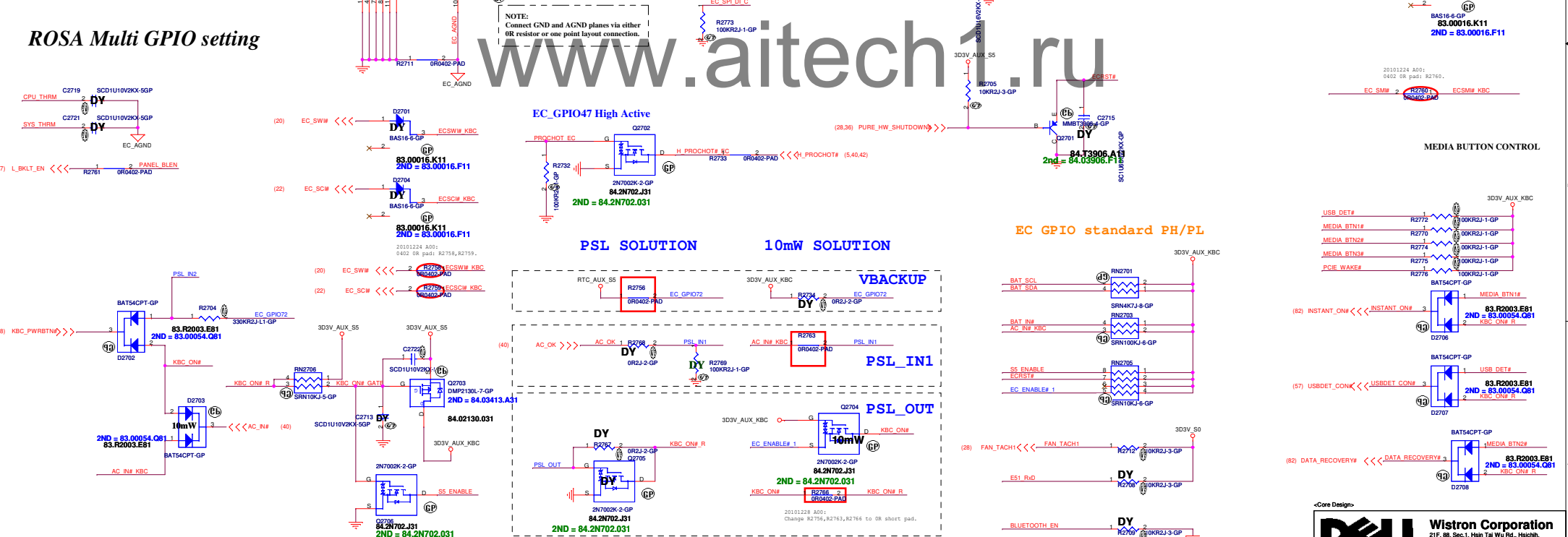
ROSA Multi GPIO setting

PCB Version A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

NOTES:
The NPCE795P GPIO/PWM outputs that are connected to LEDs have high drive buffers (20mA) and can be connected directly to the LEDs.



Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil



NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TXD.

Thermal sensor P2800

(27)

FAN1_DAC >

Layout 10 mil

For linear FAN

FUNCTION
Full-High ($\geq 2.795A$).
IC will be functioning when /FON voltage is above 1.6V.
n /FON is low (<0.4V), VOUT will be fully on
t Voltage
ut Voltage
voltage on this input pin controls the VOUT voltage by
ormula: $V_{OUT} = 1.6 \cdot V_{SET}$ When VSET is under 0.8V,
C will be shutdown
nd

U2802

R2802 0R2J-2-GP

FON#

5V_S0

FAN_VCC

FON#

GND

GND

GND

VSET

GND

G991P11U-GP

74.00991.031

2nd = 74.02793.A31

3rd = 74.05606.A71

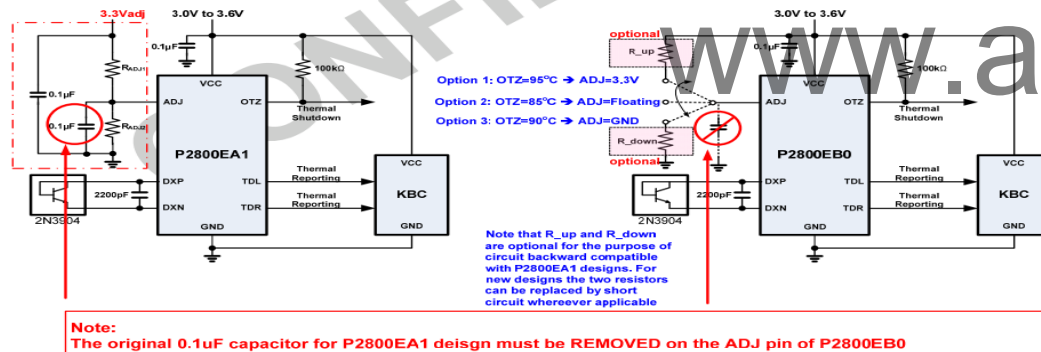
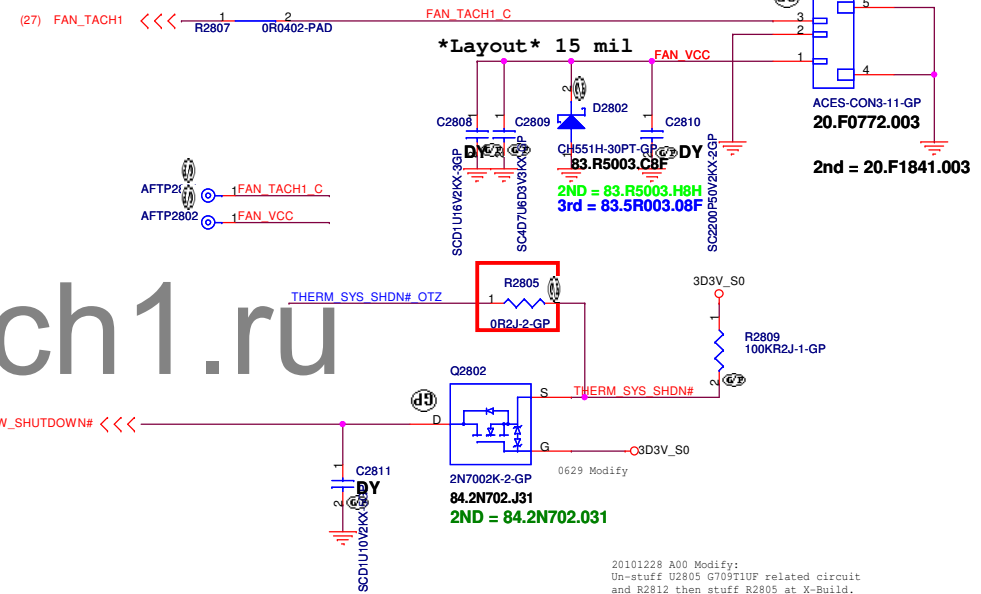
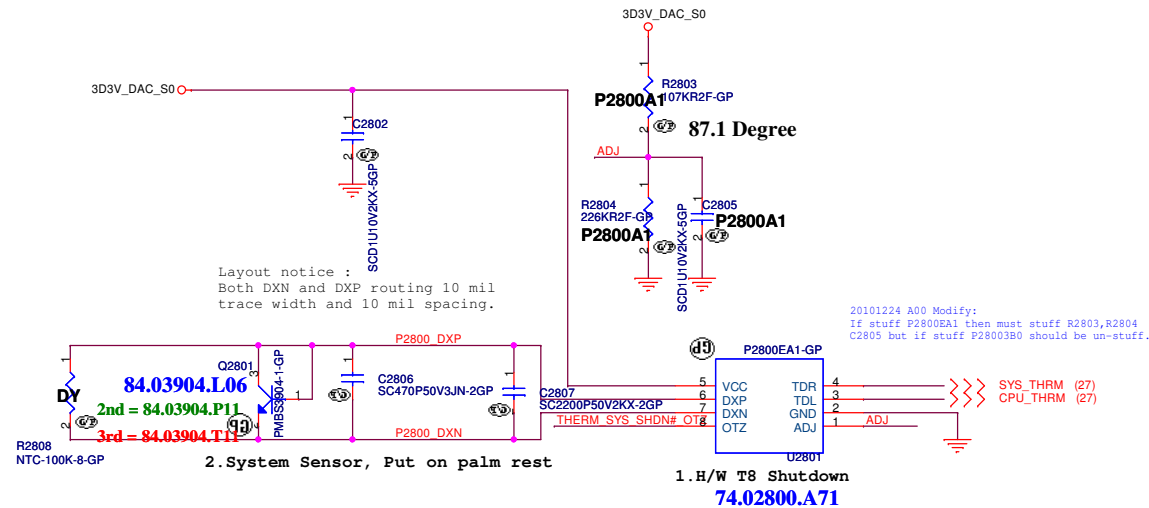
5V_S0

C2803

C2804

SC4D7U6D3VX3XX

SCD11U102KX-5G



20101228 A00 Modify:
Un-stuff U2805 G709T1UF related circuit
and R2812 then stuff R2805 at X-Build.

[illegible]

Hysteresis is 10°C for HYST = VCC, 2°C for HYST = GND.

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Title	Author	Date	Page
1. Introduction	John Doe	2023-10-27	1-5
2. Methodology	Jane Smith	2023-10-28	6-10
3. Results	Michael Johnson	2023-10-29	11-15
4. Discussion	Emily White	2023-10-30	16-20
5. Conclusion	David Brown	2023-10-31	21-25

THERMAL P2800 / Fan control

Size
A3

Document Number

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Rev
400

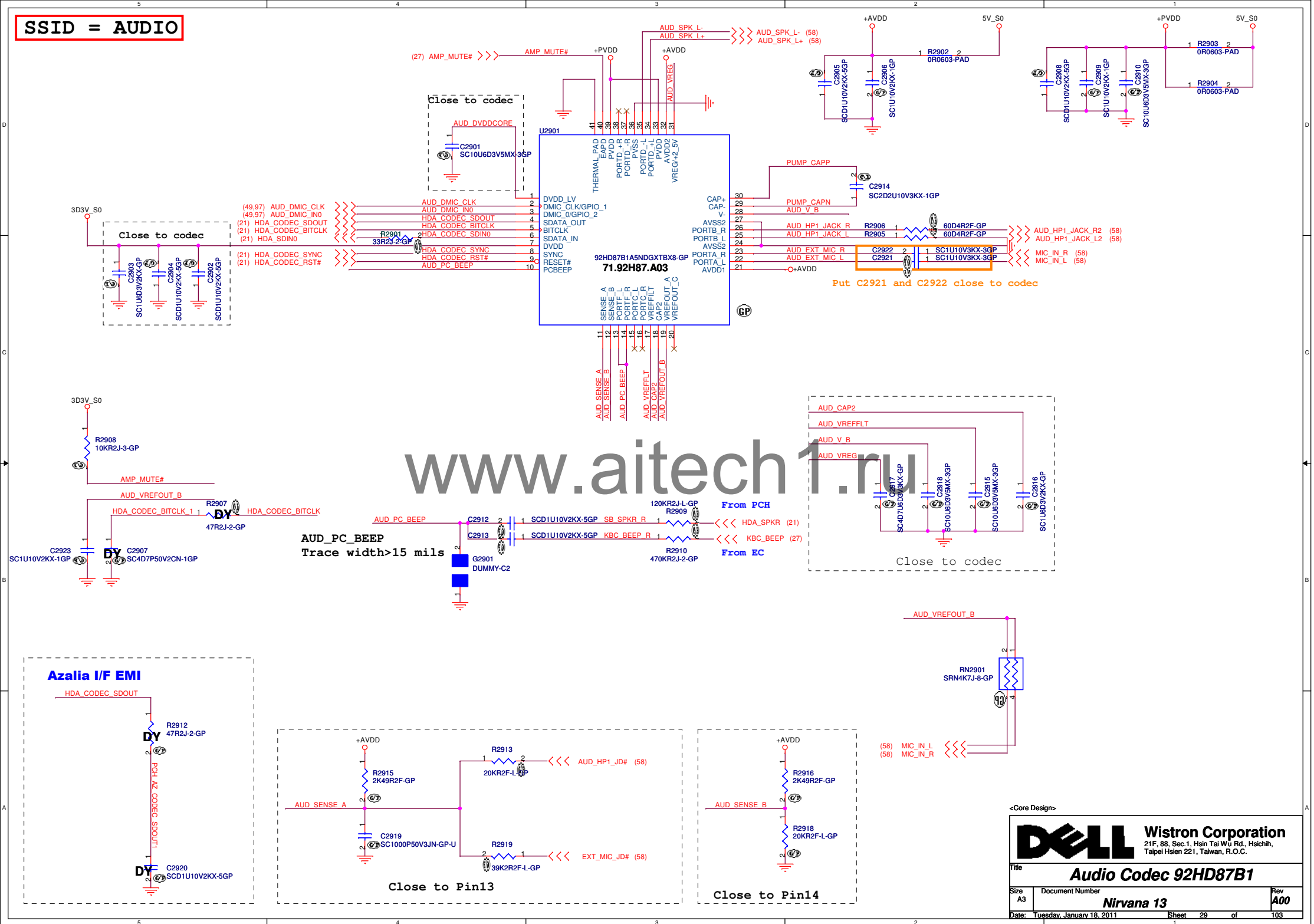
Date: Tuesday, January 18, 2011

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ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 $\pm 1\%$ Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	V _{ADJ} (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

SSID = AUDIO



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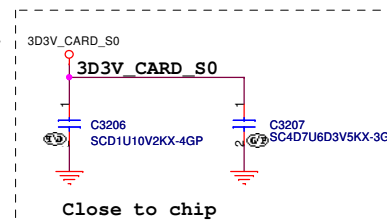
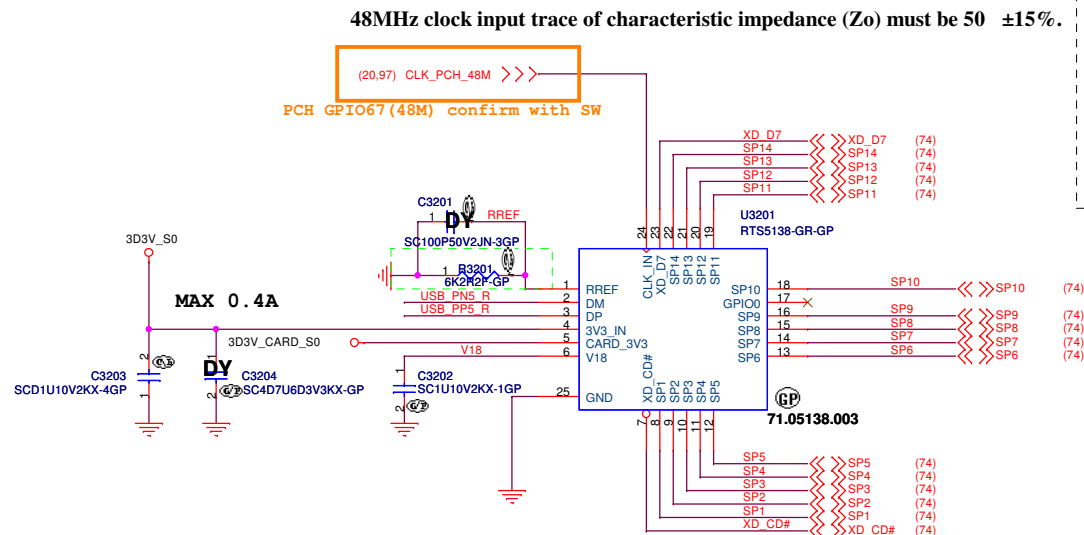
Document Number
Nirvana 13

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A00

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SSID = SDIO



PIN	TYPE	FUNCTION	RTS5138 NET
1	SD	SD-DAT2	SP13
2	SD	SD-CD/DAT3	SP12
3	MMC_PLUS	MMC-DAT4	SP11
4	SD	SD-CMD	SP10
5	MMC_PLUS	MMC-DAT5	SP9
6	SD	SD-VSS	POWER
7	SD	SD-VDD	POWER
8	MemoryStick	MS-VSS	POWER
9	MemoryStick	MS-VCC	POWER
10	MemoryStick	MS-SCLK	SP1
11	MemoryStick	MS-DATA3	SP5
12	MemoryStick	MS-INS	SP2
13	MemoryStick	MS-DATA2	SP8
14	MemoryStick	MS-DATA0	SP9
15	MemoryStick	MS-DATA1	SP12
16	MemoryStick	MS-BS	SP14
17	MemoryStick	MS-VSS	POWER
18	SD	SD-CLK	SP8
19	MMC_PLUS	MMC-DAT6	SP7
20	SD	SD-VSS	POWER
21	MMC_PLUS	MMC-DAT7	SP5
22	SD	SD-DAT0	SP4
23	SD	SD-DAT1	SP3
24	SD	SD-COM(SW)	
25	SD	SD-CD(SW)	SP6
26	XD	XD-GND	POWER
27	XD	XD-CD	XD_CD#
28	XD	XD-R/-B	SP1
29	XD	XD-RE	SP2
30	XD	XD-CE	SP3
31	XD	XD-CLE	SP4
32	XD	XD-ALE	SP5
33	XD	XD-WE	SP6
34	XD	XD-WP	SP7
35	XD	XD-GND	POWER
36	XD	XD-D0	SP8
37	XD	XD-D1	SP9
38	XD	XD-D2	SP10
39	XD	XD-D3	SP11
40	XD	XD-D4	SP12
41	XD	XD-D5	SP13
42	XD	XD-D6	SP14
43	XD	XD-D7	XD-D7
44	XD	XD-VCC	POWER
45	SD	SD-WP(SW)	SP1

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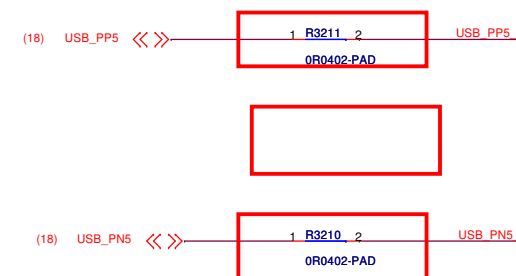
The maximum range of the PMOS output current

1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

POWER TRACE

1. RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2. RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3. RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum).
Keep the trace routing lengths as short as possible.
4. RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5. RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6. De-coupling and Bulk capacitor should place near to RTS5138 chip and Combo Socket.
7. It is recommended that use of ferrites bead on power trace.
8. Via size: Pad \geq 32 mils, Finished hole \geq 16 mils.

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Z_{diff}) is $90\Omega \pm 10\%$



20101227 A00:
Change R3210, R3211 to 0R 0402 pad.
20100104 A00:
Remove TR3201.

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Title			Card Reader RTS5138	
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A3	Nirvana 13	A00		
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Title

Size

A3

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Title

Reserved

Size A3	Document Number Nirvana 13	Rev A00
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Date: Wednesday, December 22, 2010	Sheet 34 of 103
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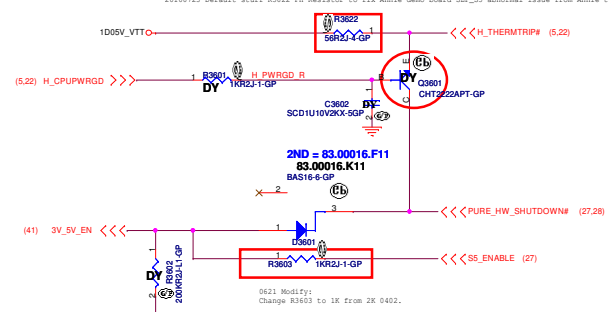
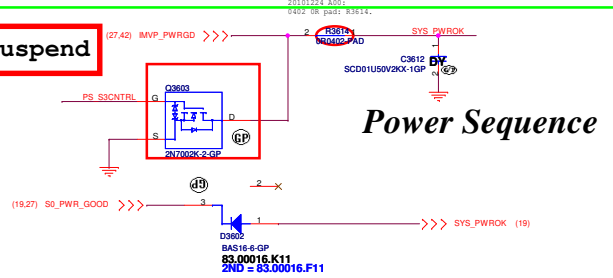
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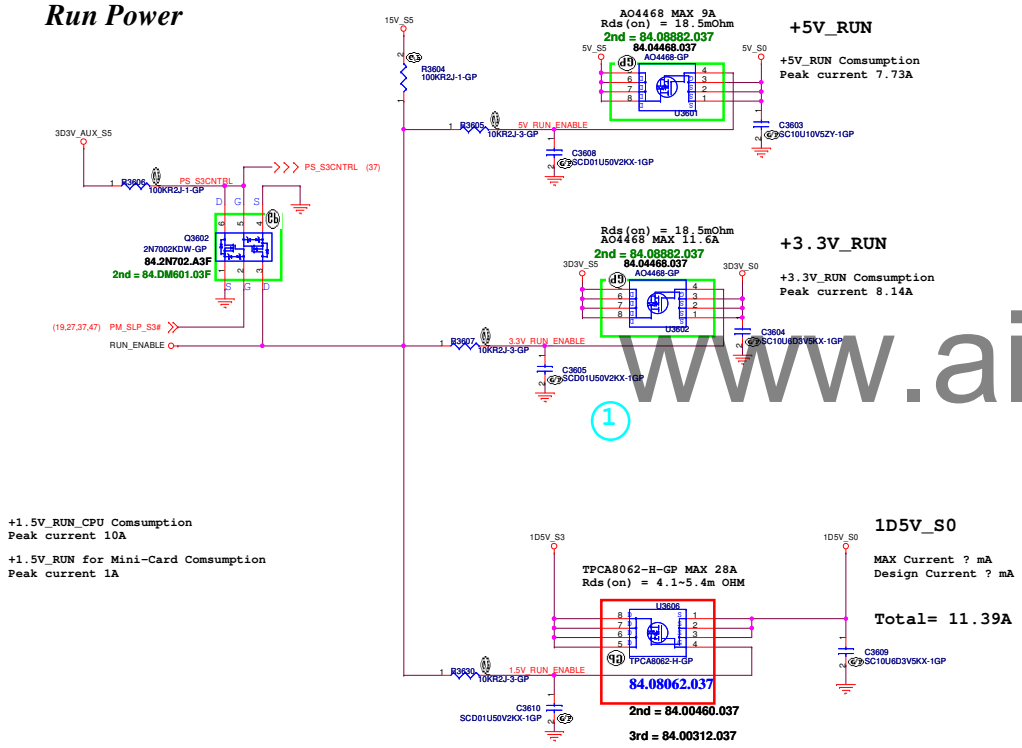
Title		Reserved	
Size	Document Number	Rev	
A3	Nirvana 13	A00	
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SSID = Reset.Suspend



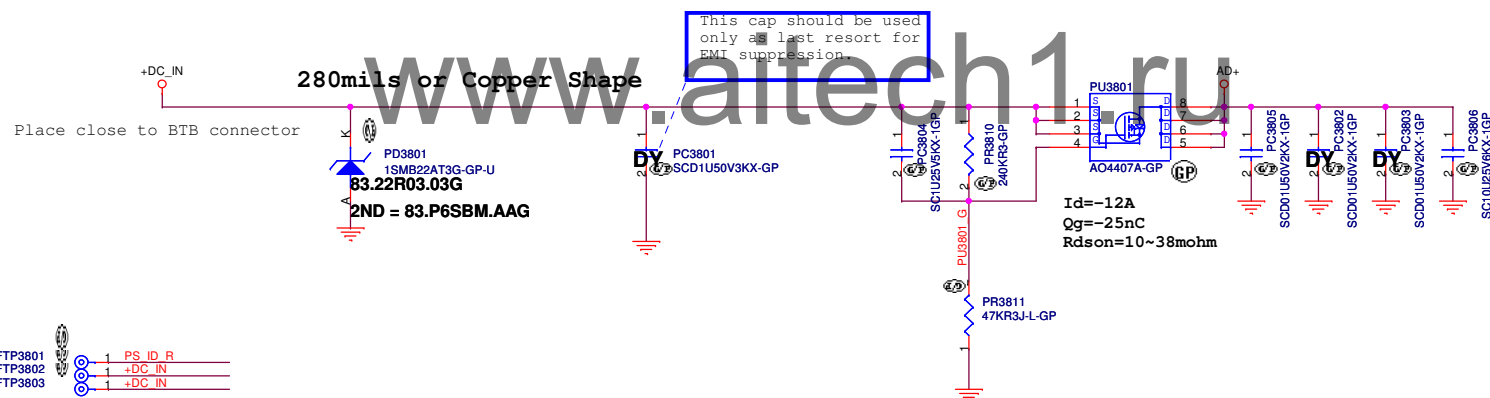
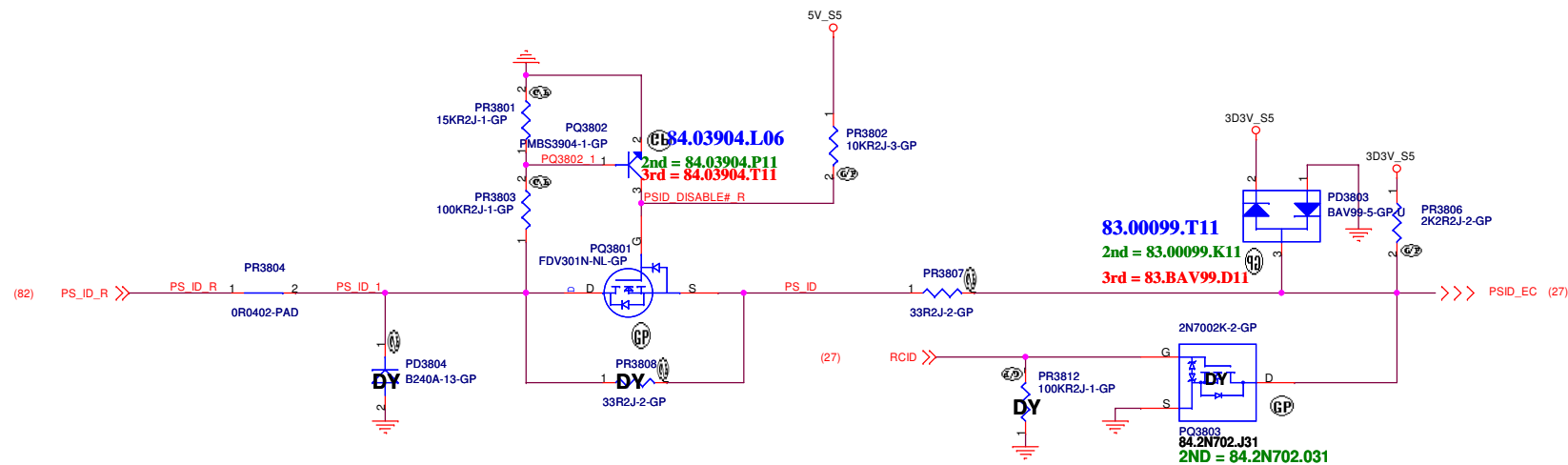
SSID = Reset.Suspend

Run Power



+1.5V_RUN_CPU Consumption
Peak current 10A

+1.5V_RUN for Mini-Card Consumption
Peak current 1A



Place close to BTB connector

280mils or Copper Shape

AFTP3801 PS_ID_R
AFTP3802 +DC_IN
AFTP3803 +DC_IN

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Title

DCIN Jack

Size
A3

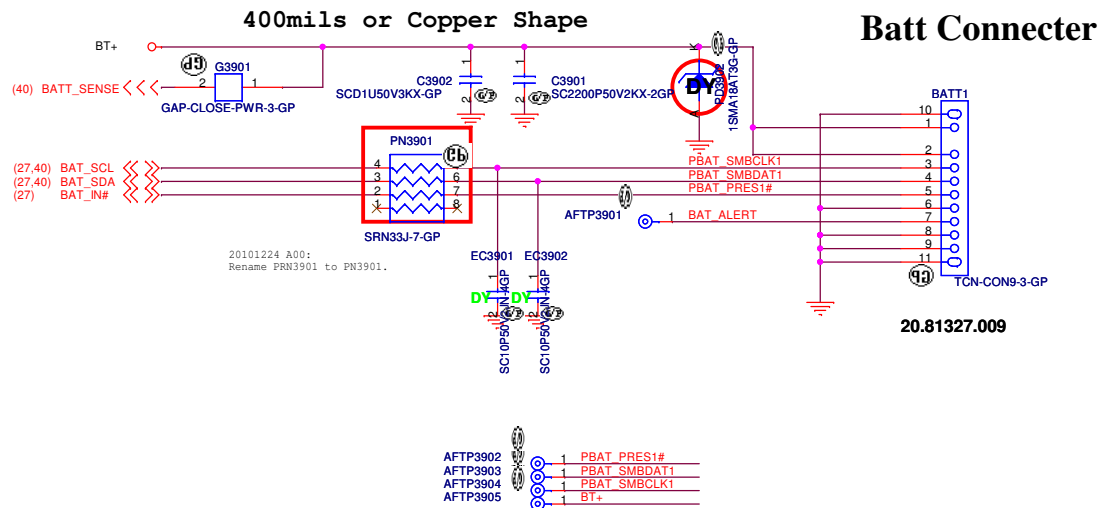
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A00

Date: Tuesday, January 18, 2011

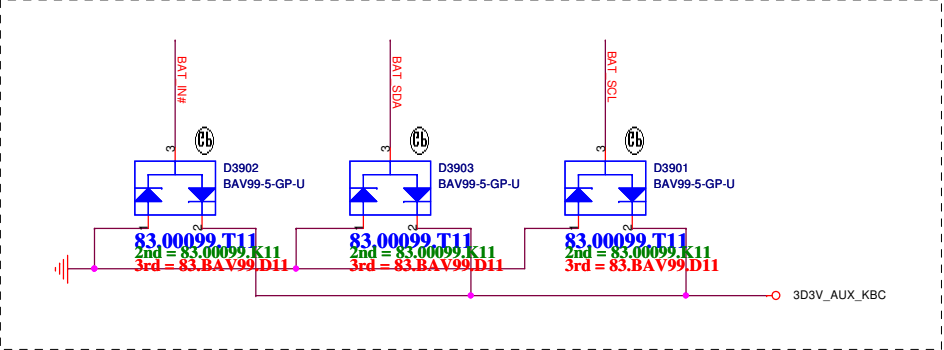
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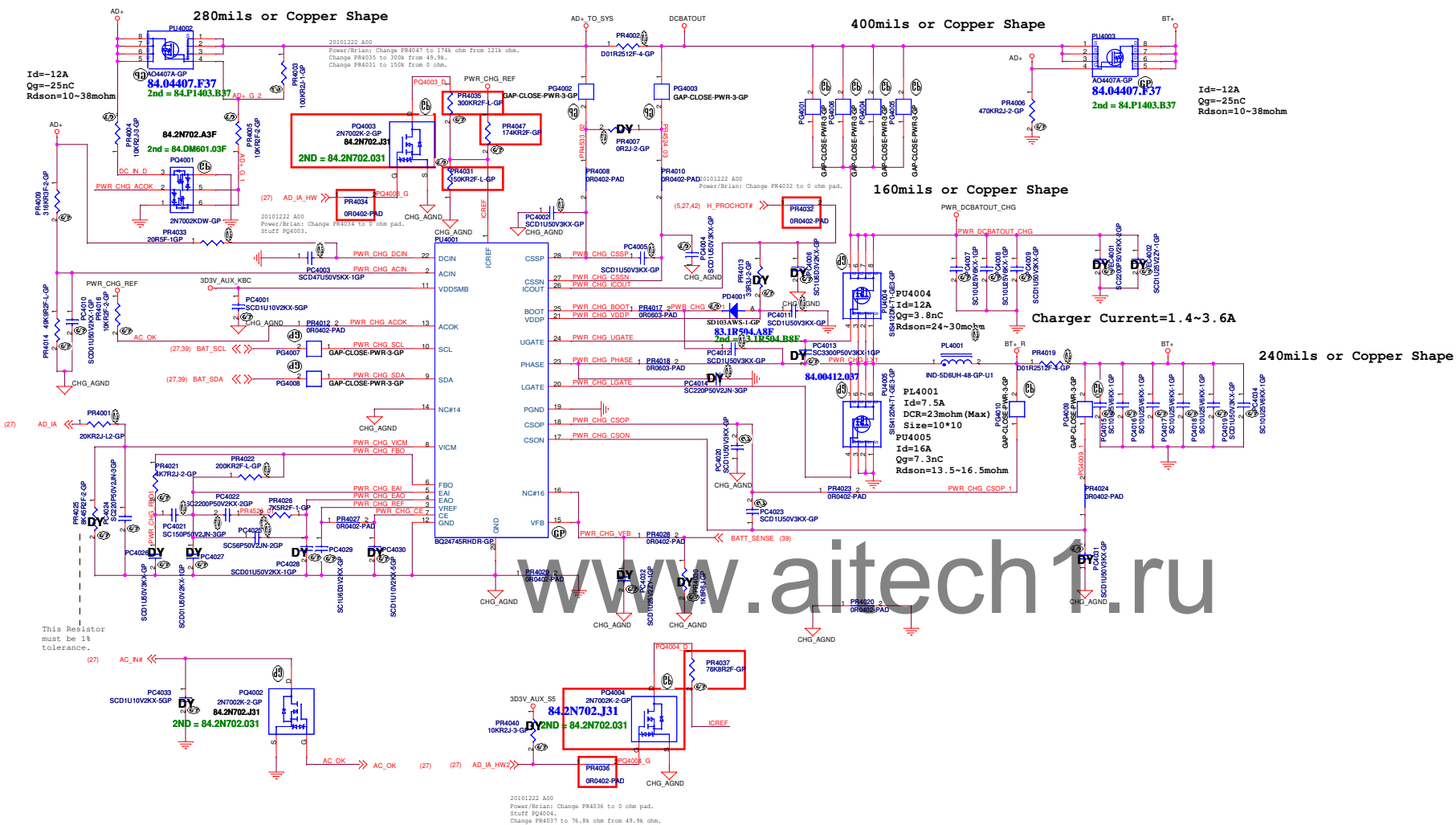
For actual location, need to be swap all pin

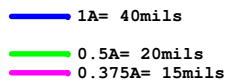
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Placement: Close to Batt Connector

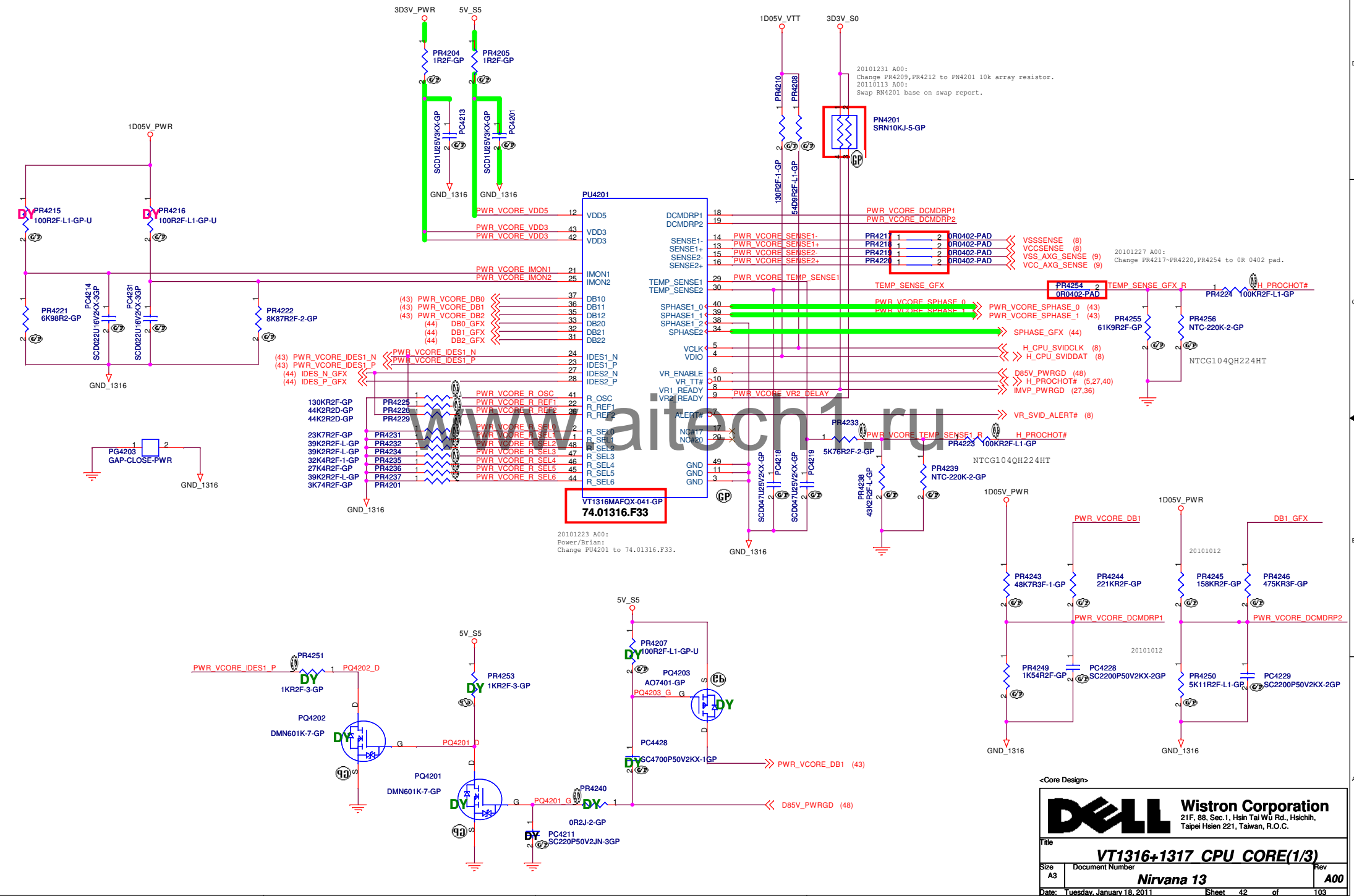


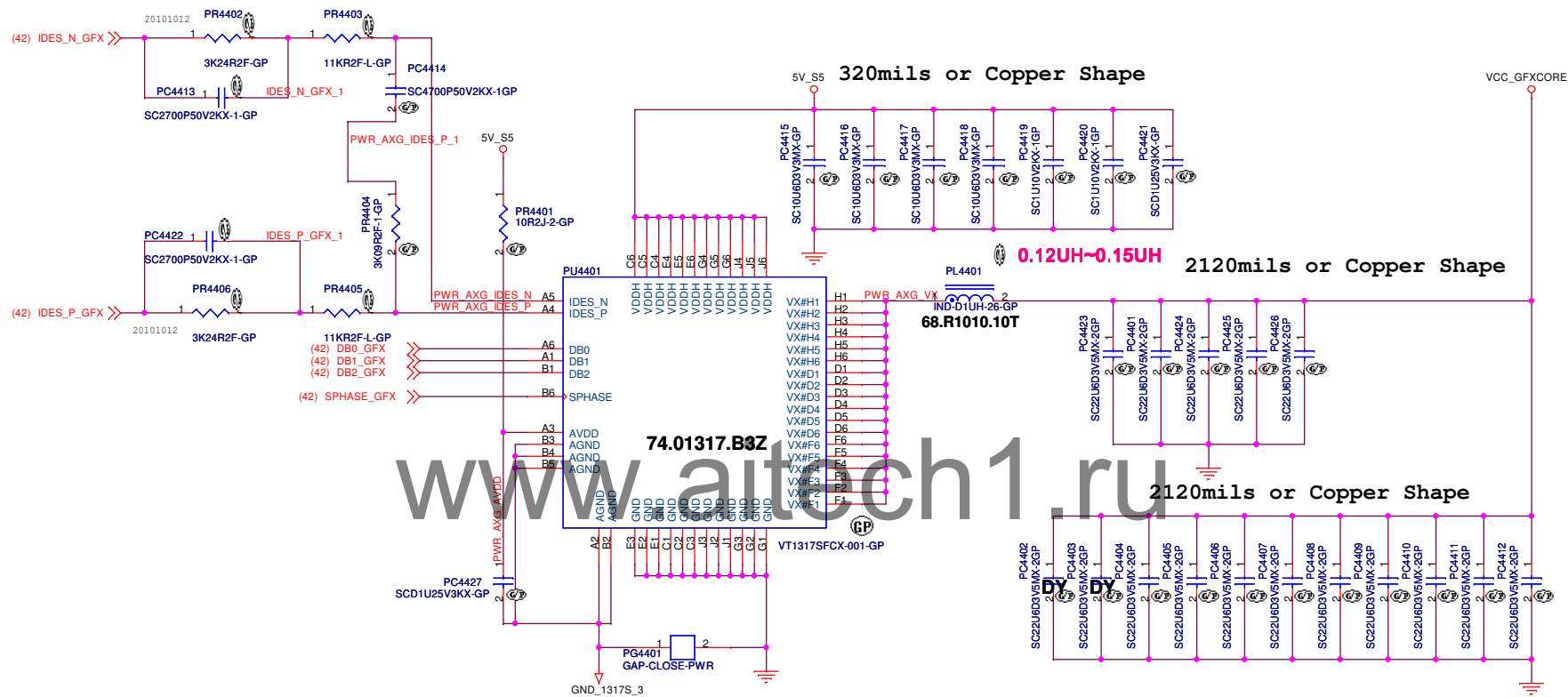
SSID = Charger





SSID = CPU.Regulator



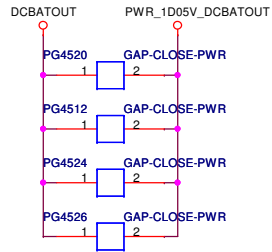


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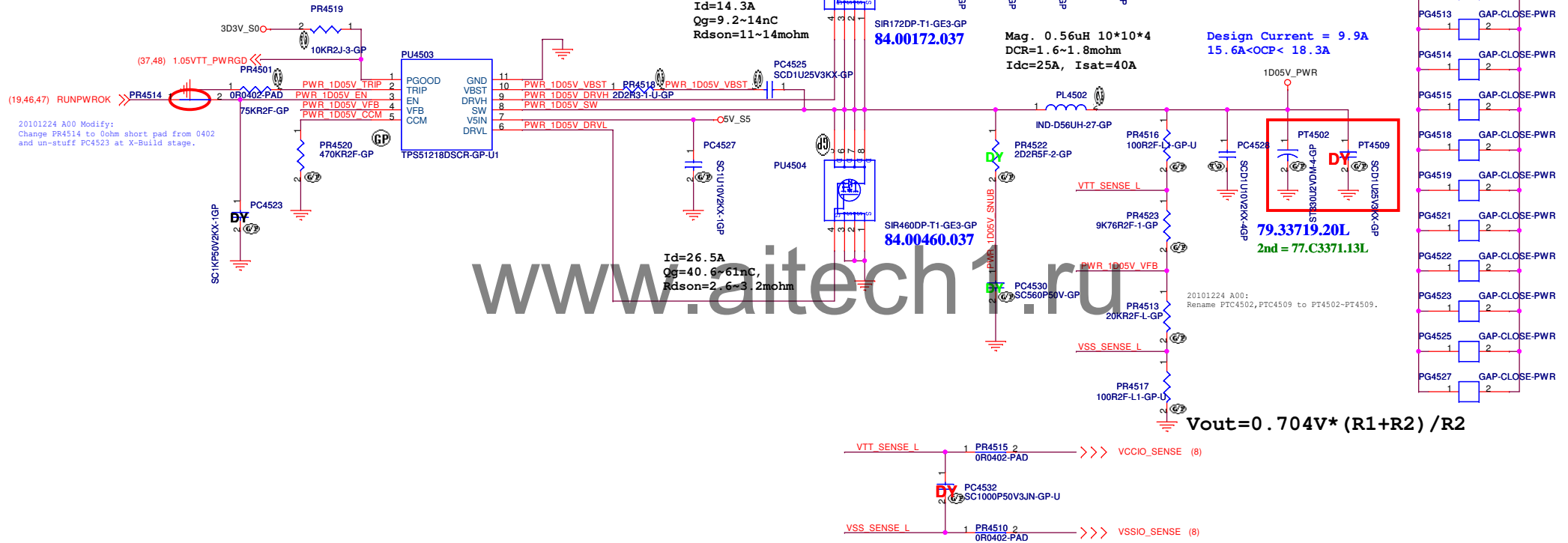


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Title		VT1316+1317 AXG CORE(3/3)	
Size	Document Number	Rev	
A3	Nirvana 13	A00	
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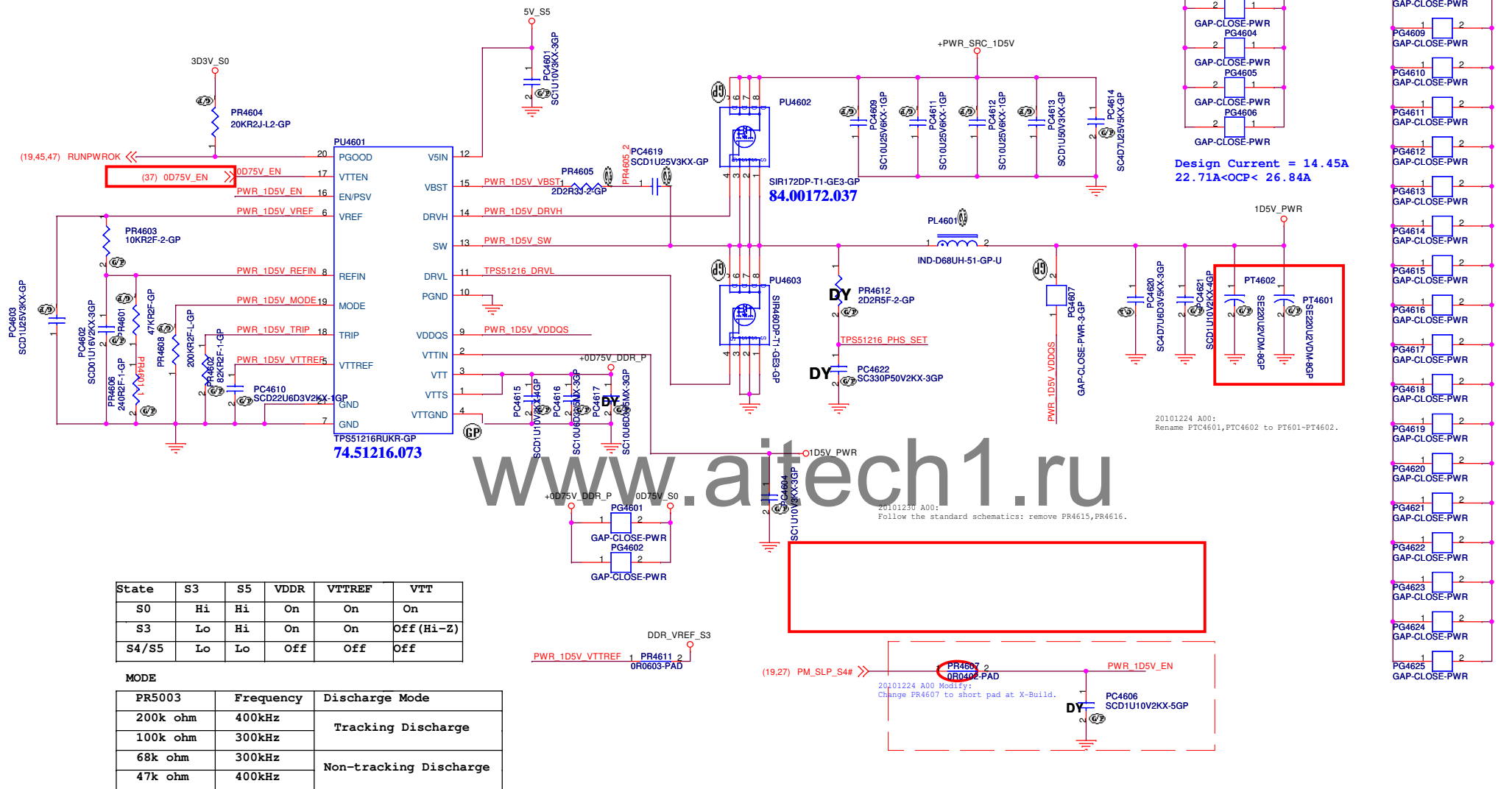


TPS51218 for 1D05V_VTT



<Core Design>

SSID = PWR.Plane.Regulator_1p5v0p75v

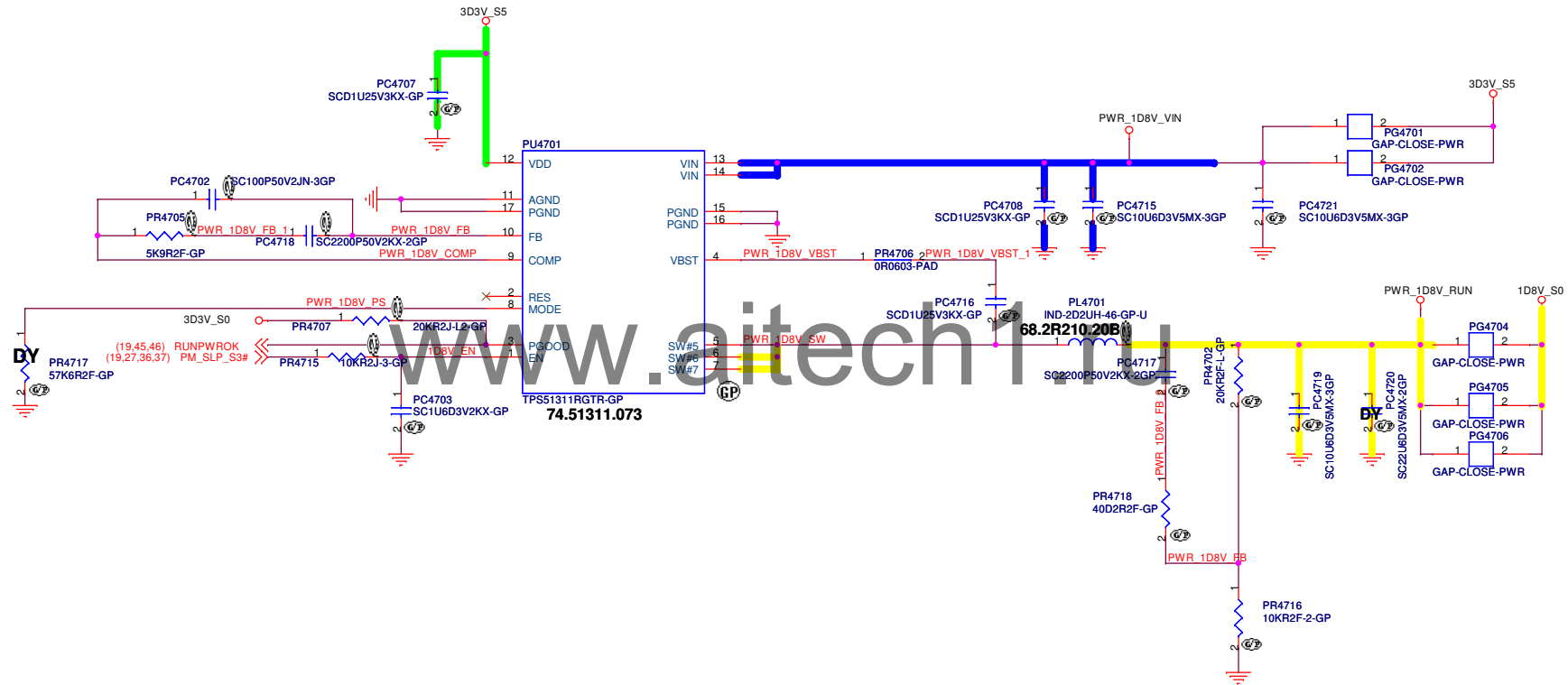


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE		
PR5003	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

SSID = PWR.Plane.Regulator_1p8v

1A= 40mils
1.5A= 60mils
0.5A= 20mils



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Title

TPS51311 +1.8V RUN

Size
A3

Document Number

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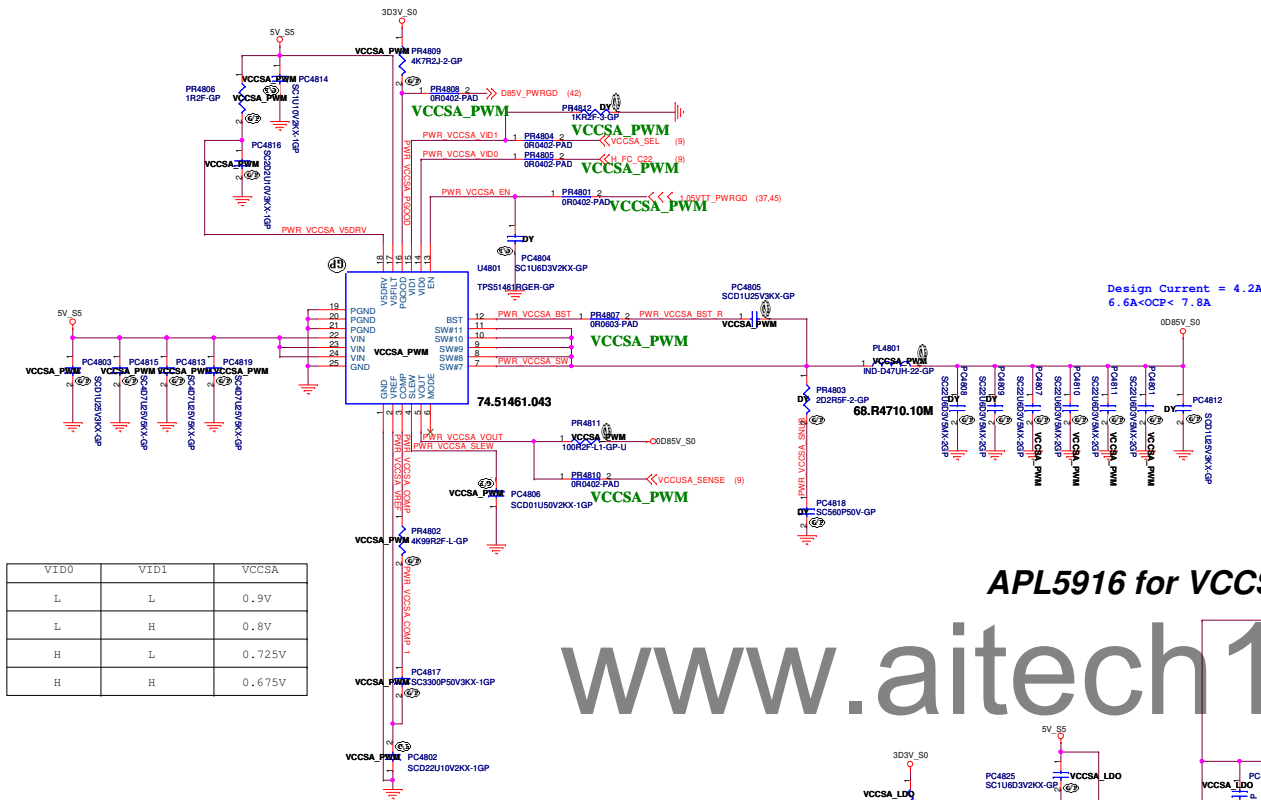
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A00

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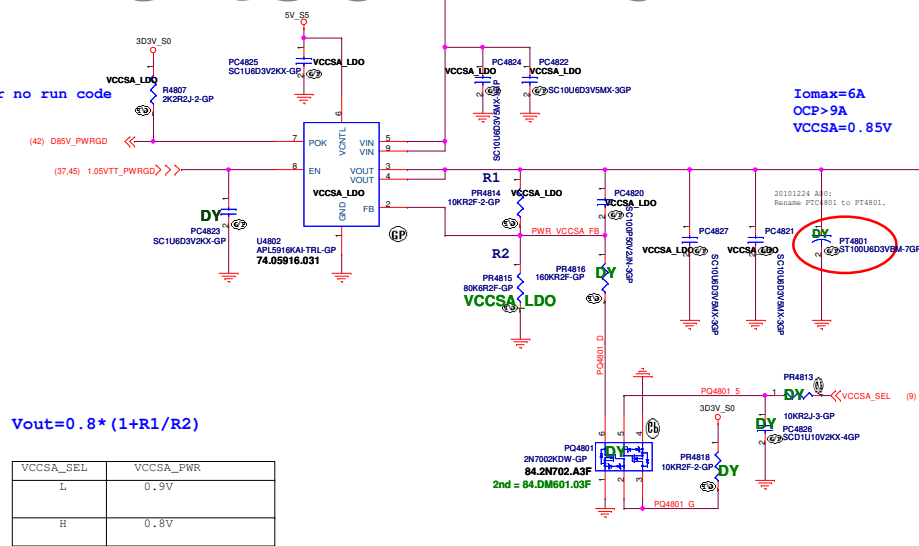
TPS51461 for VCCSA



APL5916 for VCCSA

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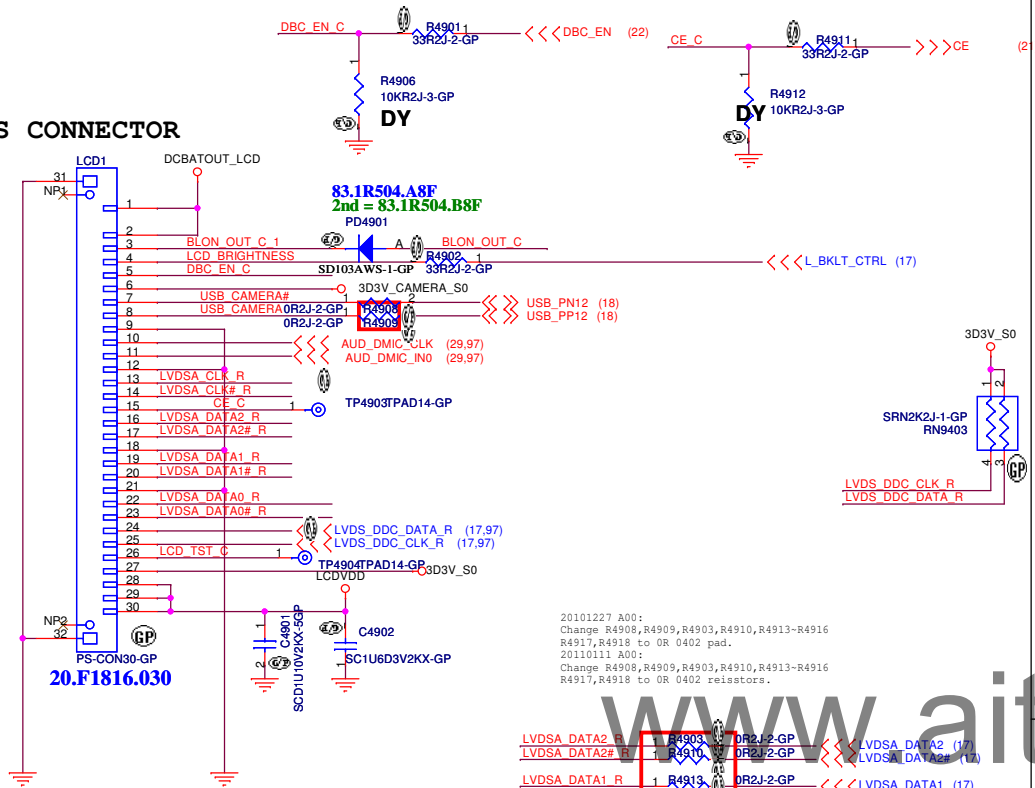
SB modify 2K2 for no run code



<Core Design>

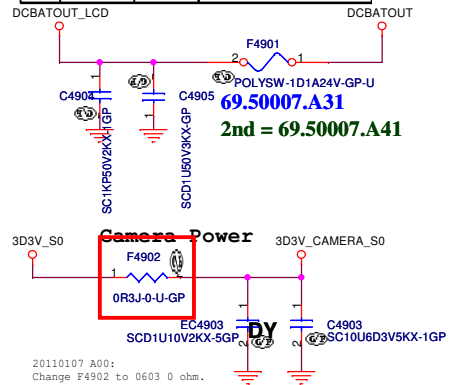
SSID = VIDEO

LVDS CONNECTOR



CAMERA and DIGITAL MIC PIN DEFINE!

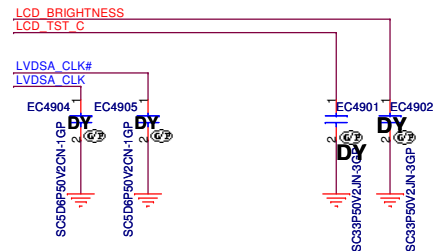
Pin No.	Name	Pin Type	Function Description
1	Debug_Loop	Power	Cable Connection to divider
2	D+	Data Pin	USB Data transmission
3	D-	Data Pin	USB Data transmission
4	USBV3.3V	Power Pin	Power Supply
5	DMIC_CLK	Data Pin	Digital MIC CLOCK
6	DMIC_DSD	GPIO	Digital MIC DSD
7	DMIC_DATA	Data Pin	Digital MIC DATA
8	GND	GPIO	System Ground



20110107 A00:
Change F4902 to 0603 0 ohm.

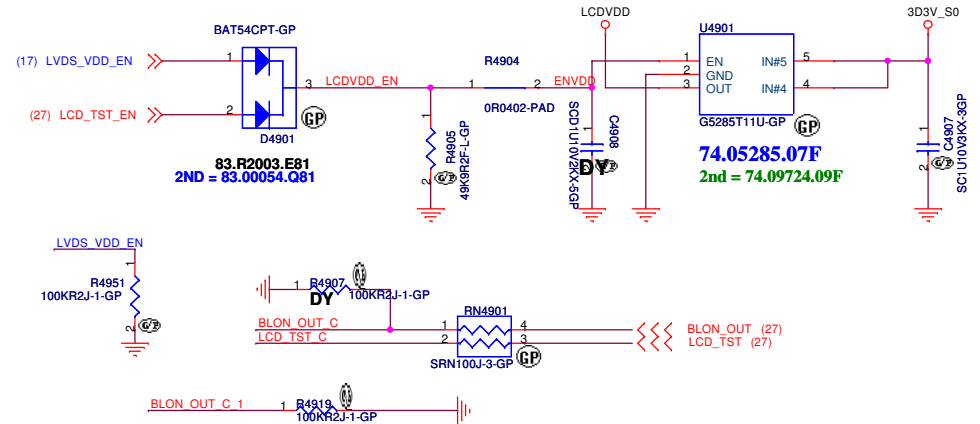
LVDSA_DATA2#_R	R4908	DR2J-2-GP	<<<	LVDSA_DATA2# (17)
LVDSA_DATA2#_R	R4910	DR2J-2-GP	<<<	LVDSA_DATA2# (17)
LVDSA_DATA1#_R	R4913	DR2J-2-GP	<<<	LVDSA_DATA1# (17)
LVDSA_DATA1#_R	R4914	DR2J-2-GP	<<<	LVDSA_DATA1# (17)
LVDSA_DATA0#_R	R4915	DR2J-2-GP	<<<	LVDSA_DATA0# (17)
LVDSA_DATA0#_R	R4916	DR2J-2-GP	<<<	LVDSA_DATA0# (17)
LVDSA_DATA2#_R	EC4906	SC10P50V2JN-4GP	<<<	LVDSA_DATA2# (17)
LVDSA_DATA2#_R	EC4907	SC10P50V2JN-4GP	<<<	LVDSA_DATA2# (17)
LVDSA_DATA1#_R	EC4908	SC10P50V2JN-4GP	<<<	LVDSA_DATA1# (17)
LVDSA_DATA1#_R	EC4909	SC10P50V2JN-4GP	<<<	LVDSA_DATA1# (17)
LVDSA_DATA0#_R	EC4910	SC10P50V2JN-4GP	<<<	LVDSA_DATA0# (17)
LVDSA_DATA0#_R	EC4911	SC10P50V2JN-4GP	<<<	LVDSA_DATA0# (17)
LVDSA_CLK#_R	R4917	DR2J-2-GP	<<<	LVDSA_CLK# (17)
LVDSA_CLK#_R	R4918	DR2J-2-GP	<<<	LVDSA_CLK# (17)

For EMI request
Close to LVDS connector



SSID = VIDEO

LCD POWER for ROSA



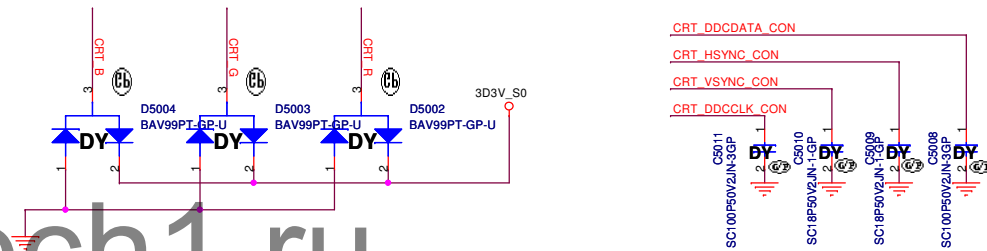
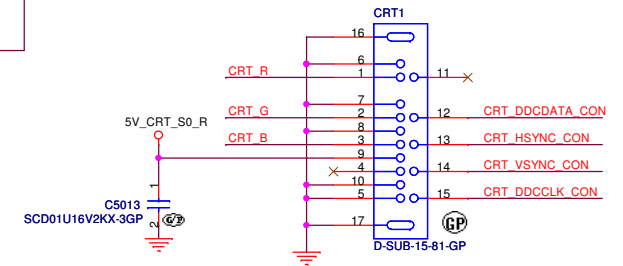
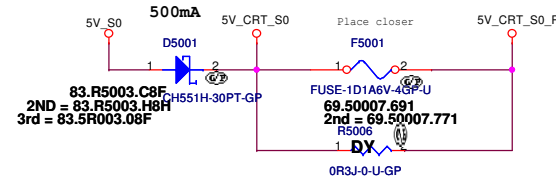
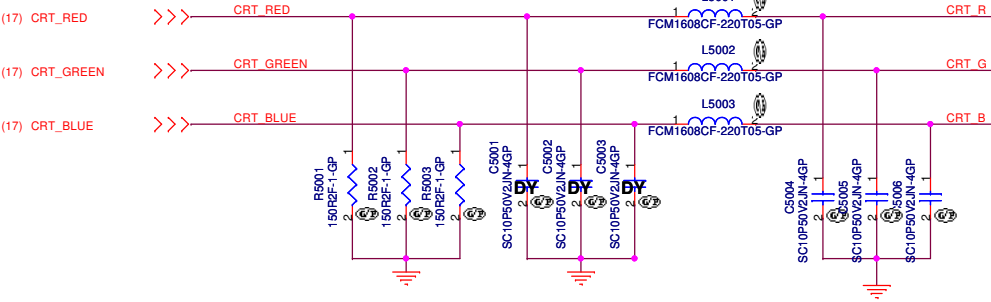
20100104 A00:
Remove TR4902.

<Core Design>



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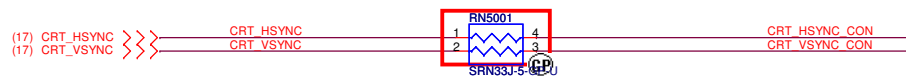
Title			
LCD/Inverter Connector			
Size A3	Document Number	Rev	
	Nirvana 13		A00
Date:	Tuesday, January 18, 2011	Sheet 49 of	103



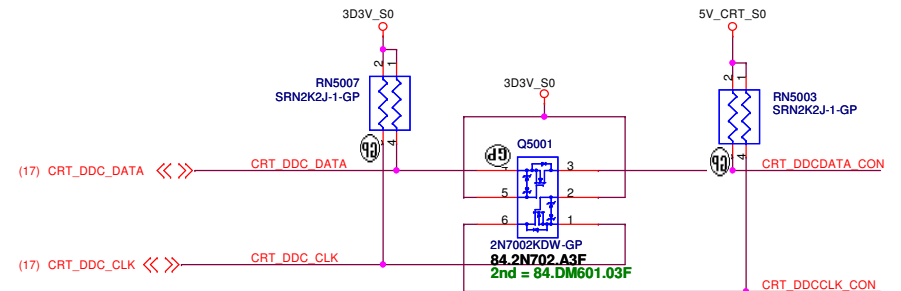
www.aitech1.ru

CRT DDCCDATA & DDCCCLK level shift

CRT Hsync & Vsync level shift



20101231 A00:
Change R5004, R5005 to RN5001 33 ohm array resistor.



<Core Design>

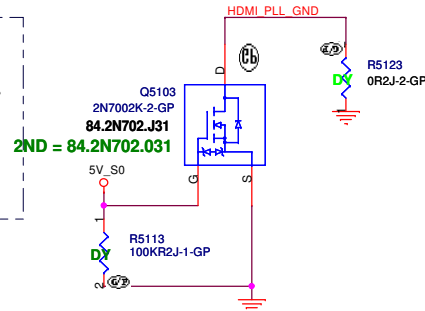
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size A3	Document Number	Rev A00
Nirvana 13		
Date: Tuesday, January 18, 2011	Sheet 50	of 103

SSID = VIDEO

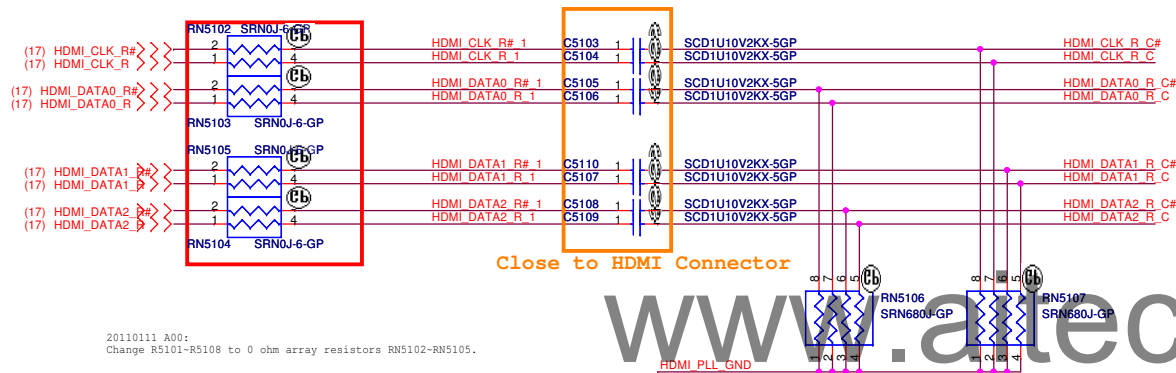
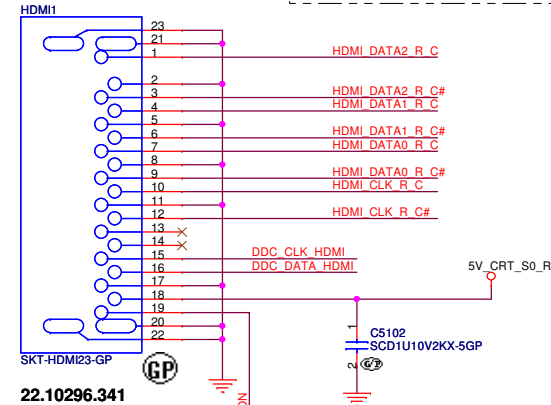
HDMI Level Shifter & CONNECTOR

Removed LEVEL SHIFTER base on DELL feedback spec.
(No support 220MHZ deep color mode, so can be removed
HDMI LEVEL SHIFTER circuit.



HDMI CONN

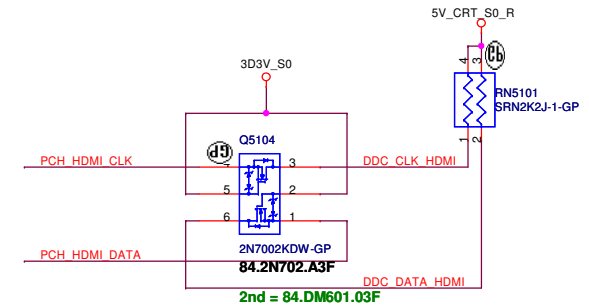
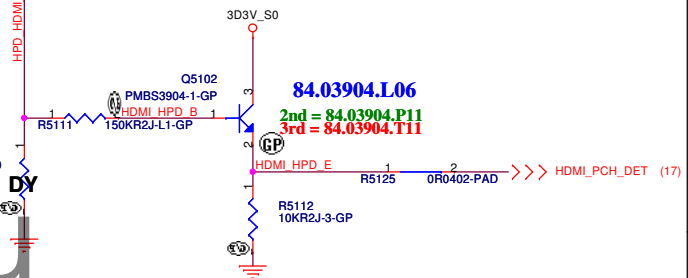
Removed HDMI_IN# CIRCUIT
connect to KBC GPIO.



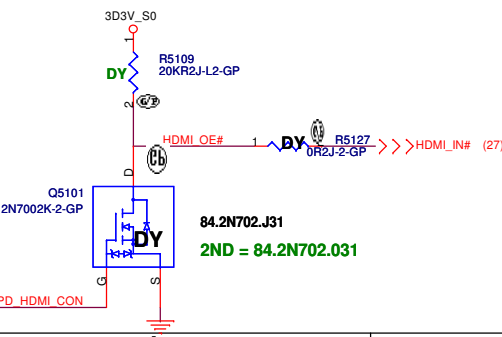
Close to HDMI Connector

www.aitech1.ru

20100723 Swap RN5106 and RN5107 base in the swap report.
suggestion to stuff 680-ohm for UMA.



Already PH on PCH side.(RN1706)



Routing Guidelines:


CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

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<Core Design>



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Title

Reserved

Size A3	Document Number Nirvana 13	Rev A00
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Title

LVDS Switch

Size
A3

Document Number

Nirvana 13

Rev

A00


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Title

Reserved

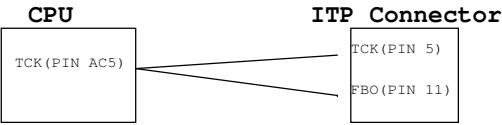
Size	Document Number	Rev
A3	Nirvana 13	A00

Date: Wednesday, December 22, 2010	Sheet 54 of 103
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SSID = User.Interface

ITP Connector

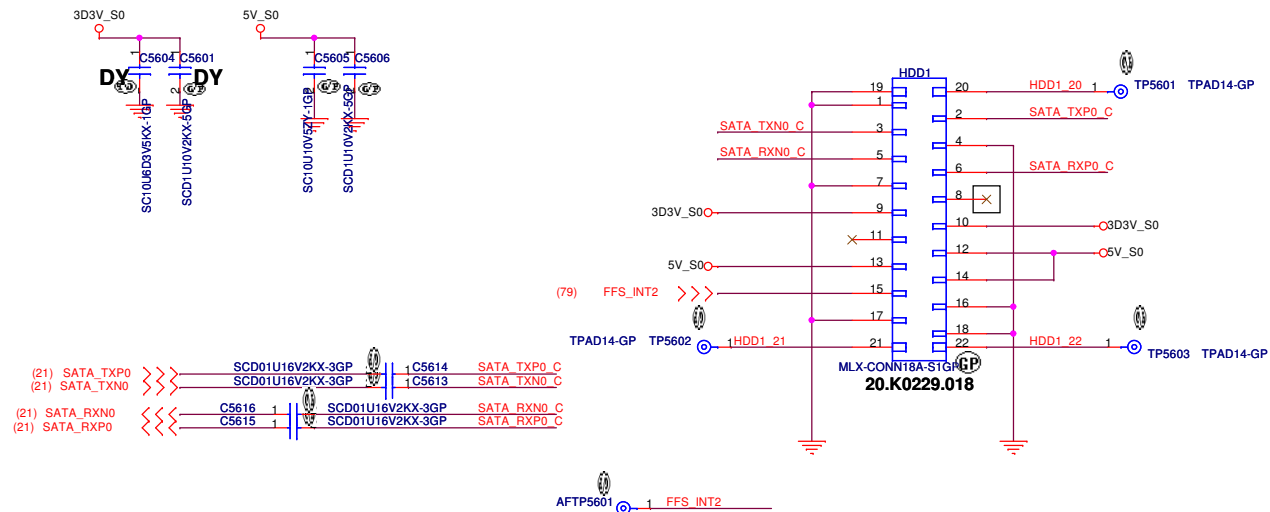
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



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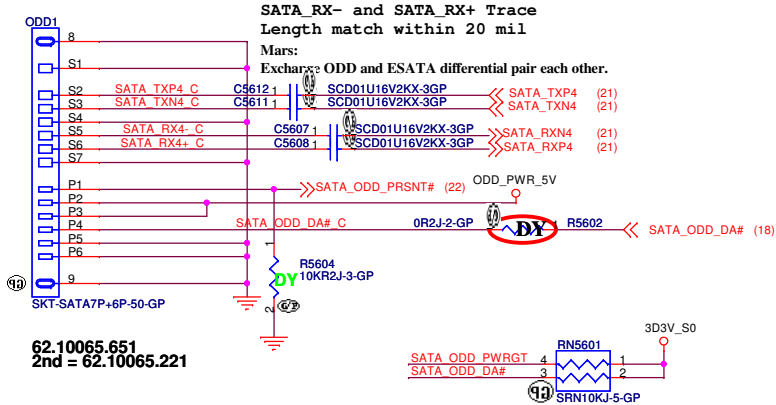
SSID = SATA

SATA HDD Connector

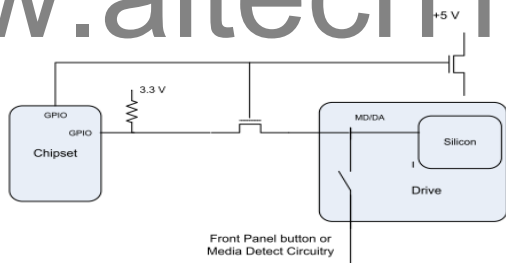


www.aitech1.ru

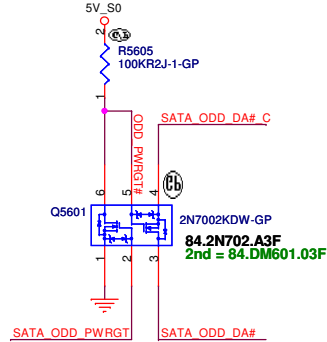
ODD Connector



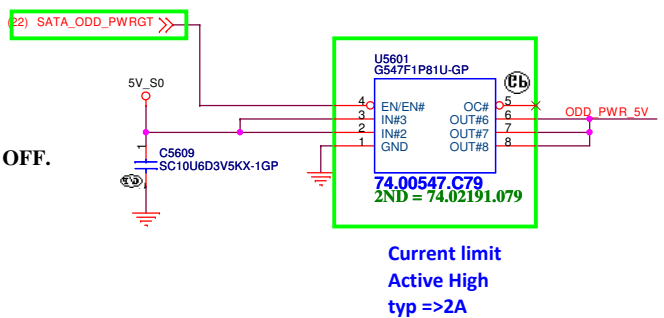
SUPPORT ZERO SATA ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

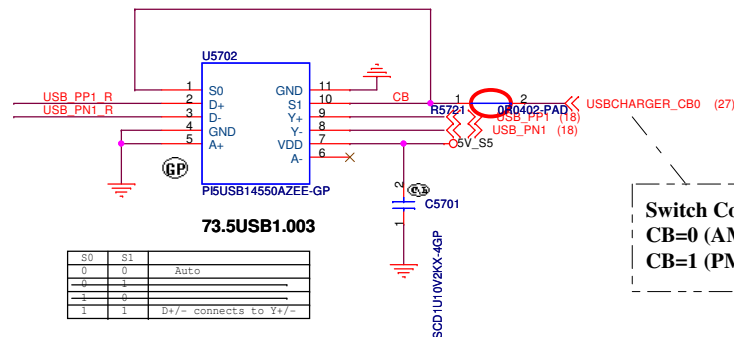


SATA Zero Power ODD



SSID = ESATA

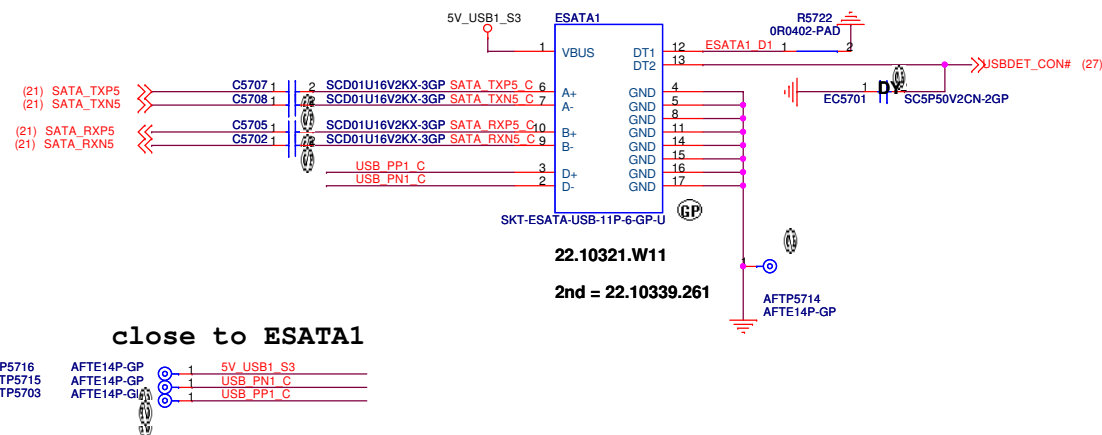
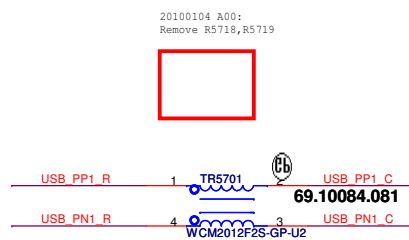
USB CHARGER



Switch Control Bit:
CB=0 (AM):auto detection charger identification active.
CB=1 (PM):connect DP/DM to TDP/TDM.

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ESATA CONN



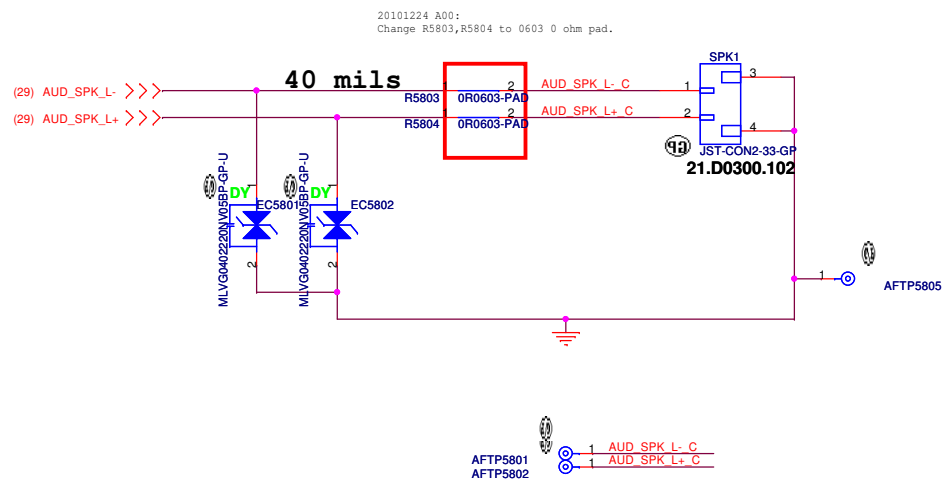
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Taipei Hsien 221, Taiwan, R.O.C.

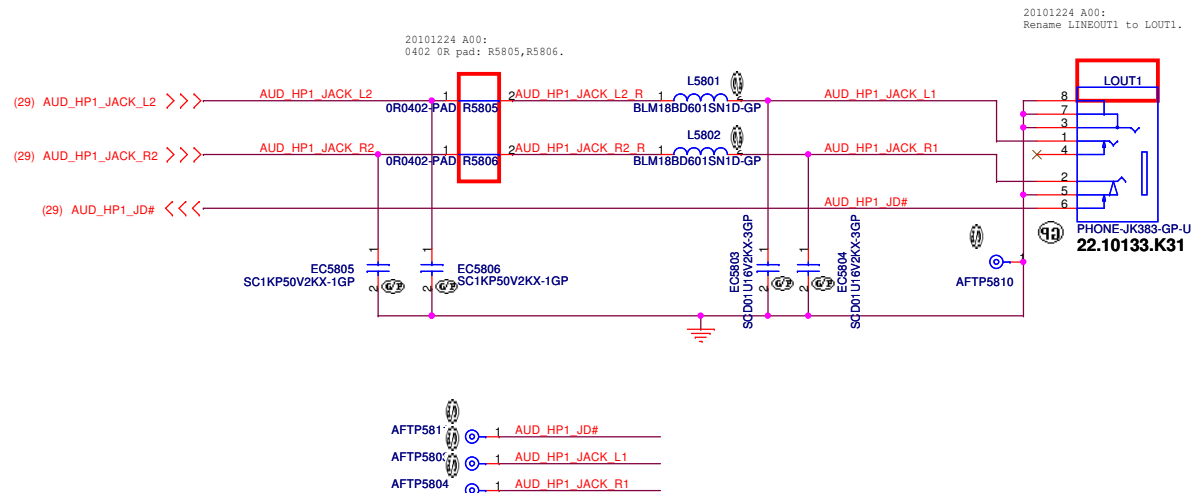
Title
USB/ESATA
Size A3 Document Number
Nirvana 13 Rev
A00
Date: Tuesday, January 18, 2011 Sheet 57 of 103

SSID = AUDIO

Speaker Connector

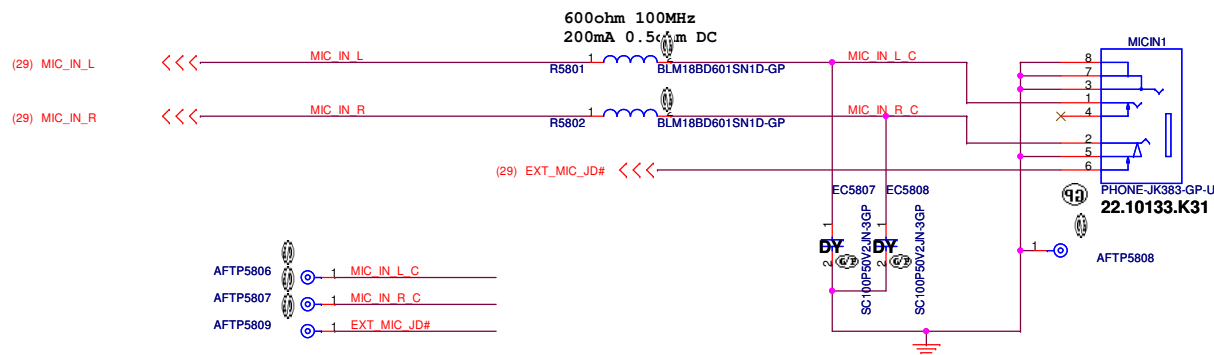


LINE OUT



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MIC IN



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Title

Audio Jack

Size
A3

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<Core Design>

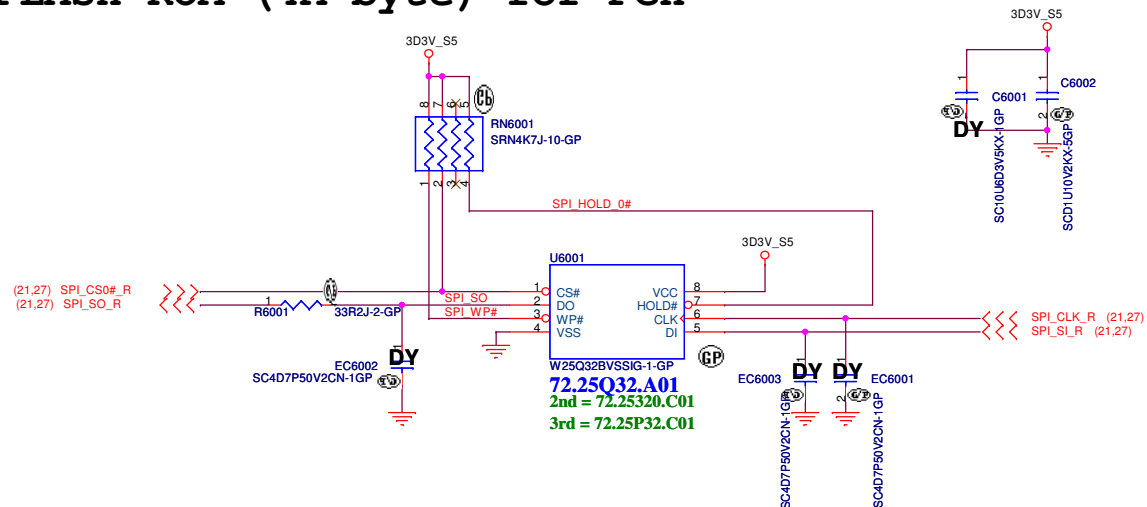


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Taipei Hsien 221, Taiwan, R.O.C.

Title			Reserved		
Size	Document Number				Rev
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Date: Wednesday, December 22, 2010			Sheet	59	of 103

SSID = Flash.ROM

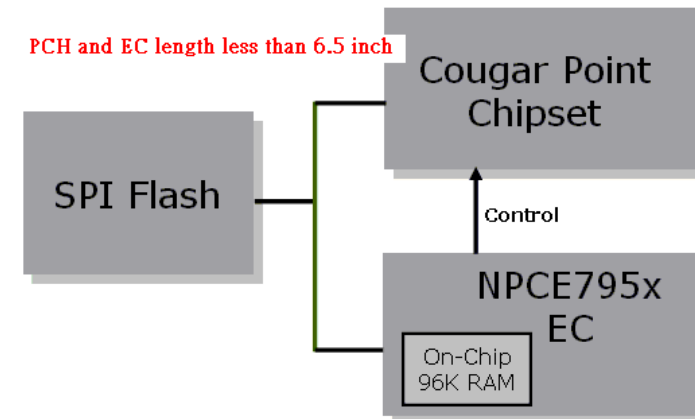
SPI FLASH ROM (4M byte) for PCH



Notes:

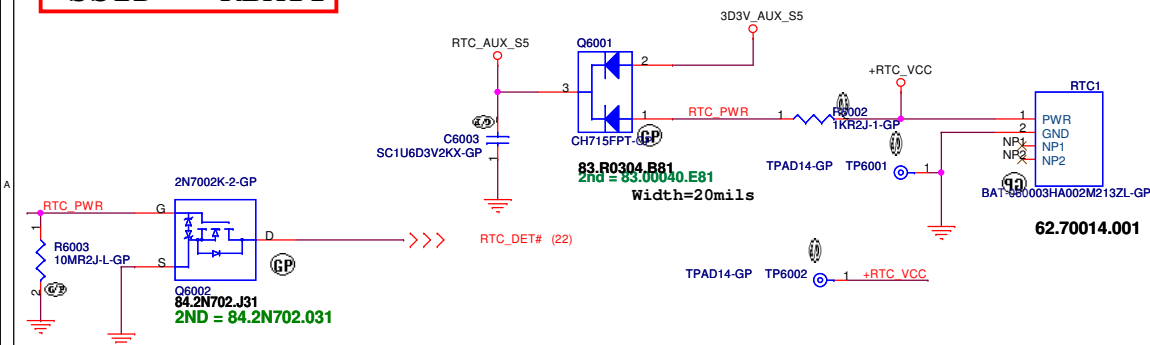
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

PCH and EC length less than 6.5 inch



Priority	Wistron P/N	Manufacturer	Vendor P/N
1	72.25Q32.A01	WINDBOND	W25Q32BV-SIG
2	72.2532A.C01	MXIC	MX25Q3206EM-126
3	72.25P32.C01	WINONIX	M25P32-VMW6F

SSID = RBATT



<Core Design>

DELL

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Title

Flash/RTC

Size
A

Document Number

Nirvana 13

Rev

Date: Tuesday, January 18, 2011

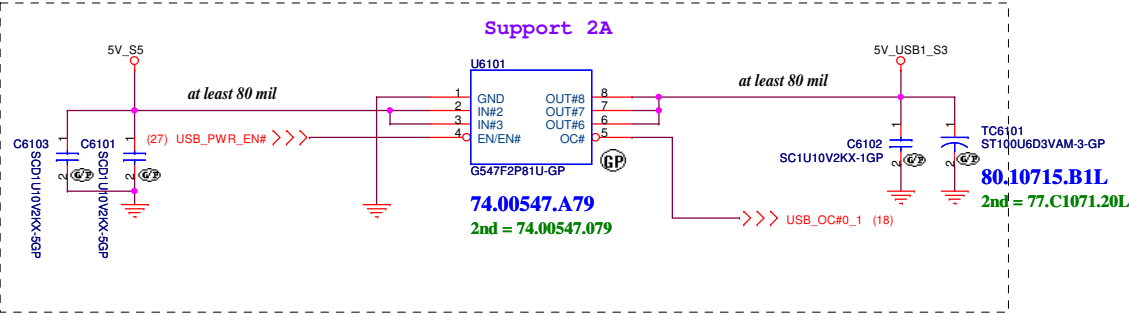
Sheet 6

103

SSID = USB

Close to ESATA Combo connector

USB POWER SW
Main G547F2P81U-GP P/N:74.00547.A79



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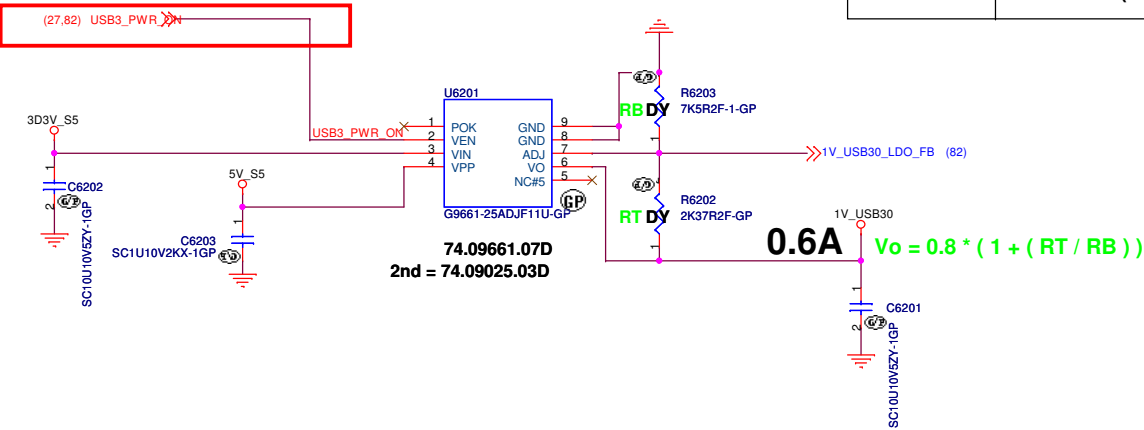


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Title			USB2.0 Power SW	
Size	Document Number		Rev	
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1V_USB30 LDO

20101227 A00:
Change R6205 to 0R 0402 pad.
20101228 A00:
VGA_TSTRM change to USB_PWR_EN.
20101229 A00:
Remove R6205, R6201 and rename USB3_PWR_ON from USB_PWR_EN.

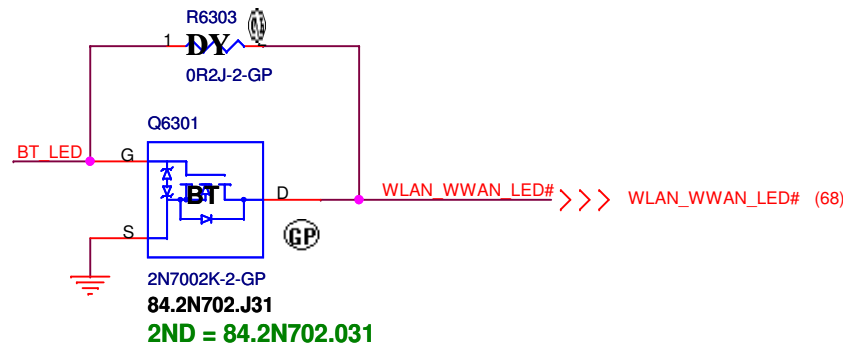
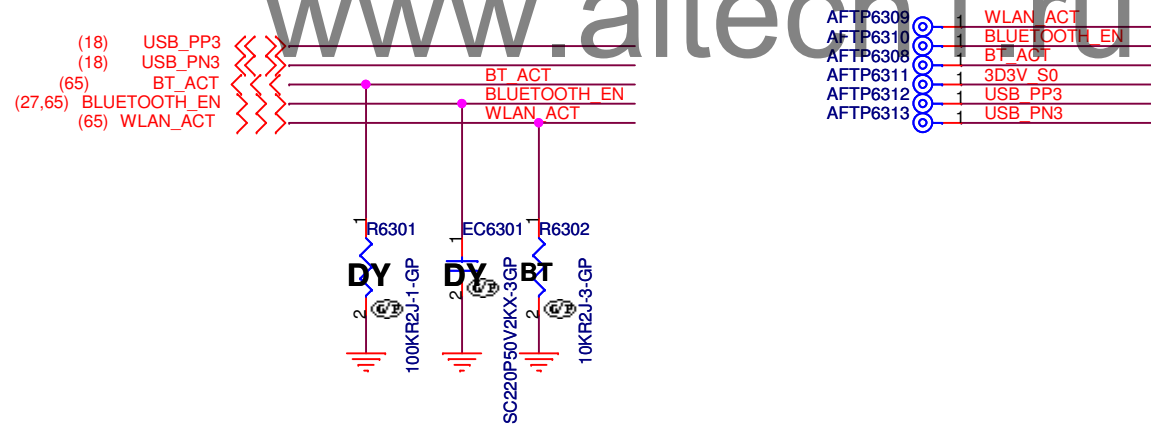
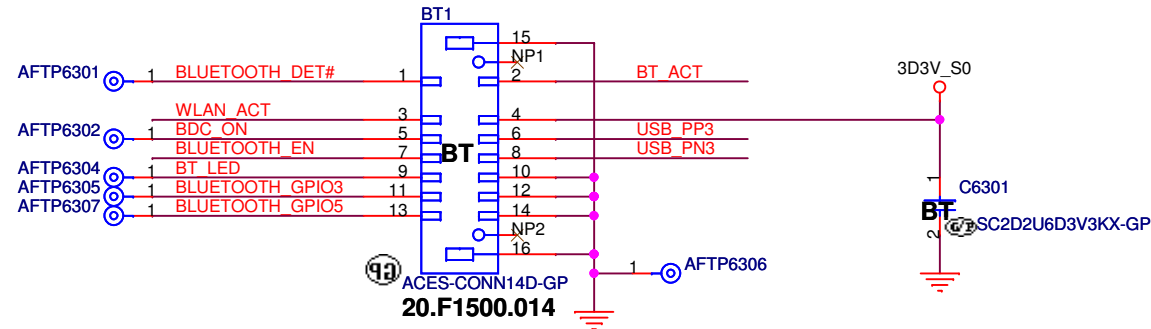


USB3.0 Host	RT (R6202)	RB (R6203)	VOUT
NEC	2.37k ohm (64.23715.6DL)	7.5k ohm (64.75015.6DL)	1.05V
TI	11.8k ohm (64.11825.6DL)	30.9k ohm (64.30925.6DL)	1.1V

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SSID = User.Interface

Bluetooth Module



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Title

Bluetooth

Size
A4

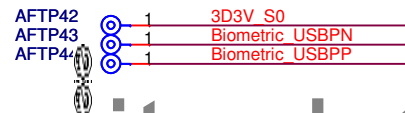
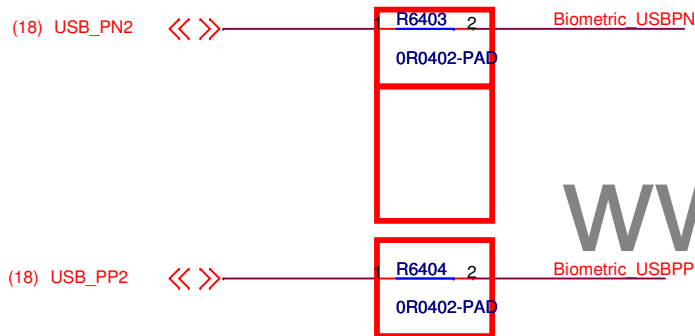
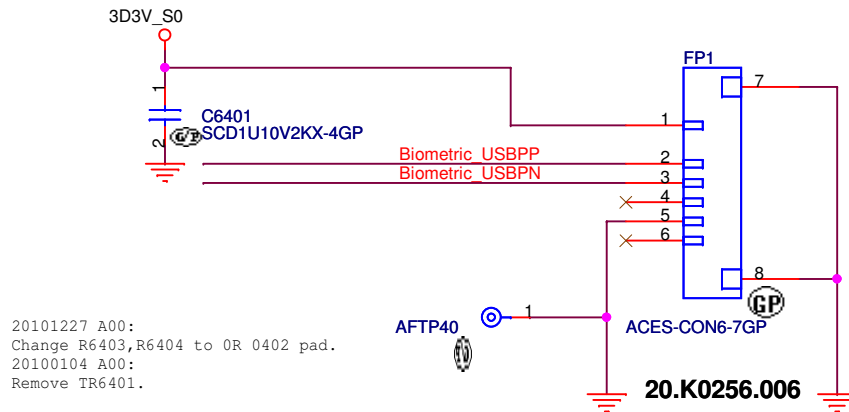
Document Number

Nirvana 13

Rev
A00


Date: Tuesday, January 18, 2011

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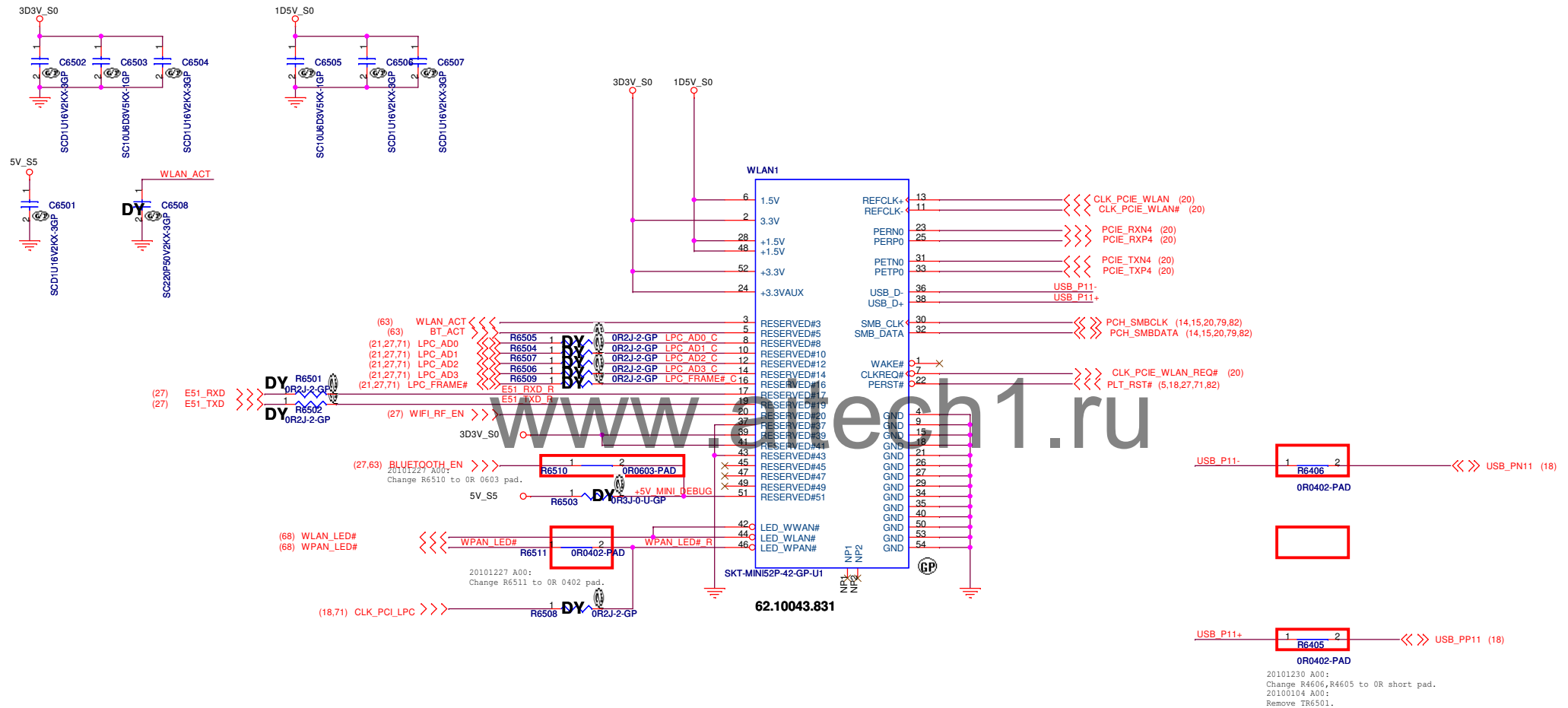
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Finger Printer Conn	
Size A4	Document Number Nirvana 13		Rev A00
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SSID = Wireless


Mini Card Connector(802.11a/b/g/n)



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Title

Size
A3

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Nirvana 13

Date: Wednesday, December 22, 2010

Rev
A00

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Title

Reserved

Size
A4

Document Number

Nirvana 13

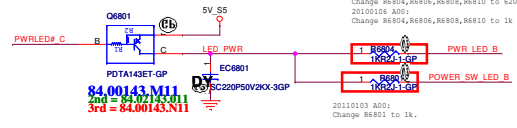
Rev
A00

Date: Wednesday, December 22, 2010

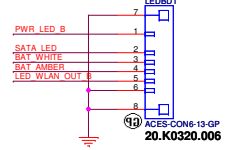
Sheet 67 of 103

SSID = User.Interface

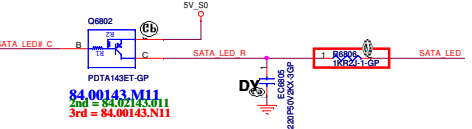
Power LED(White)



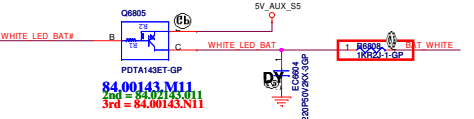
LED BD Connector



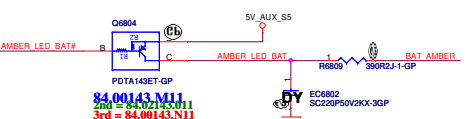
SATA HDD LED(White)



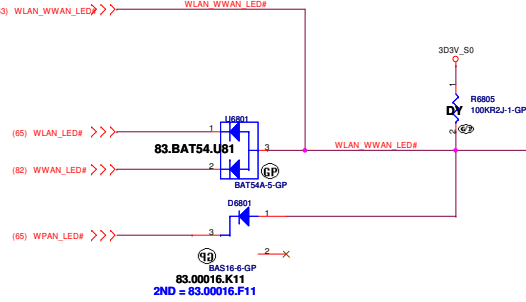
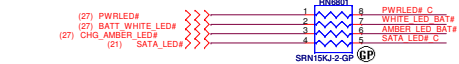
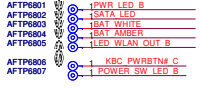
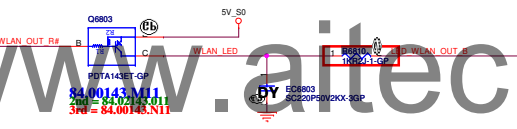
Battery LED1(White)



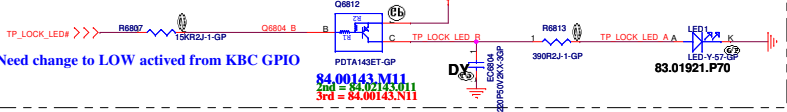
Battery LED2 (Amber)



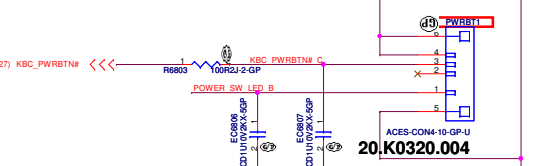
WLAN LED (White)



TPLOCK LED



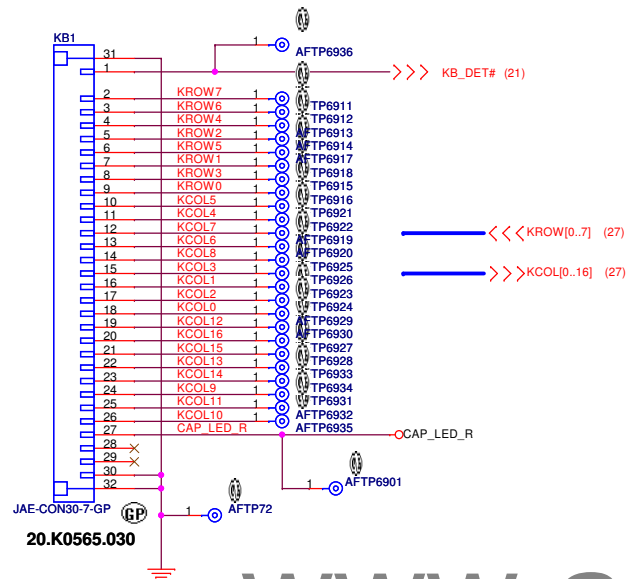
Power button LED(White)



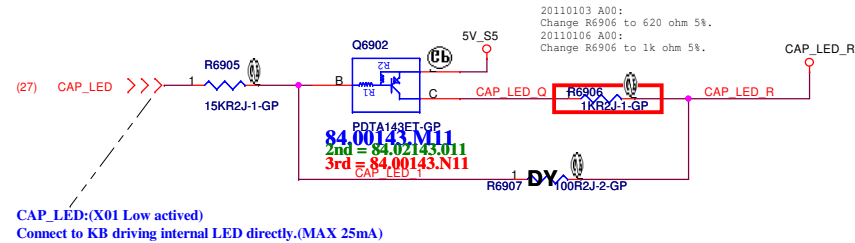
SSID = KBC

Internal KeyBoard Connector

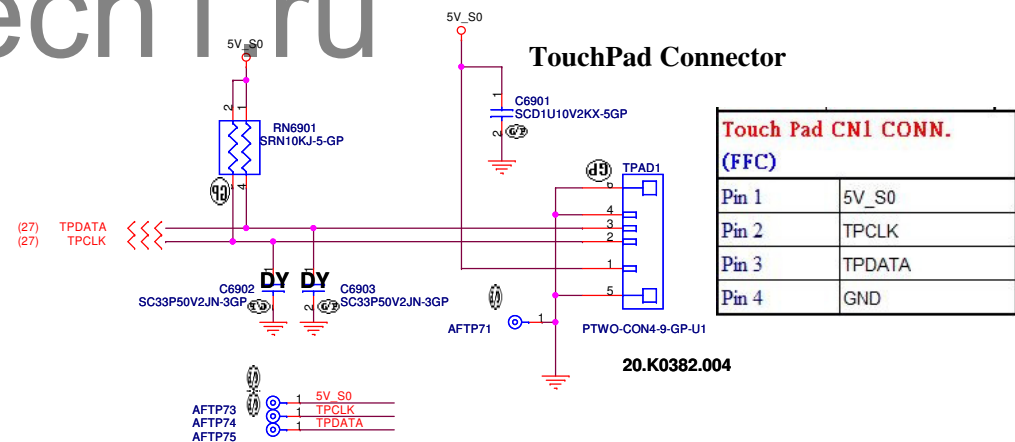
PIN No.	Description
1	Diag_Loop=GPIO_1(TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND



CAP LED CONTROL

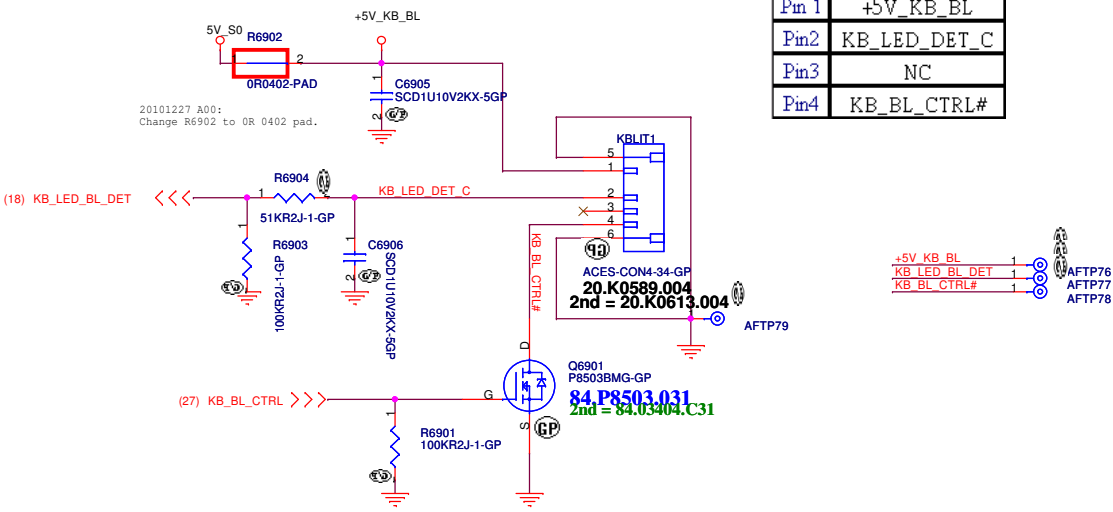


TouchPad LOCKED



KB Backlight Connector

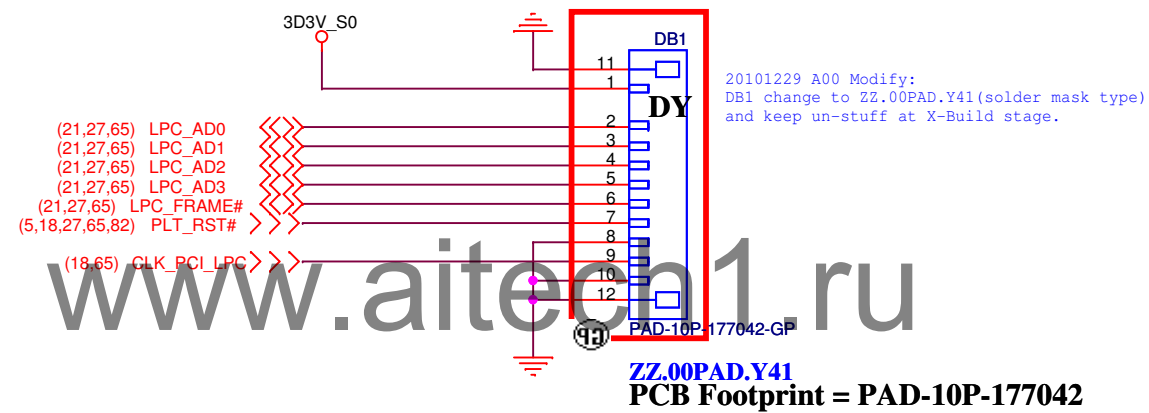
MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin 2	KB_LED_DET_C
Pin 3	NC
Pin 4	KB_BL_CTRL#



<Core Design>

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File: **Key Board/Touch Pad/Media Board**
Size: A3 Document Number: **Nirvana 13** Rev: **A00**
Date: Tuesday, January 18, 2011 Sheet: 69 of 103



<Core Design>



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Title

Dubug CONN

Size
A4

Document Number

Nirvana 13

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Date: Tuesday, January 18, 2011

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<Core Design>



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Title

Reserved

Size A3	Document Number Nirvana 13	Rev A00
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Date: Wednesday, December 22, 2010	Sheet 72 of 103
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

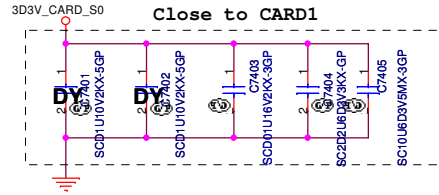
Title

Reserved

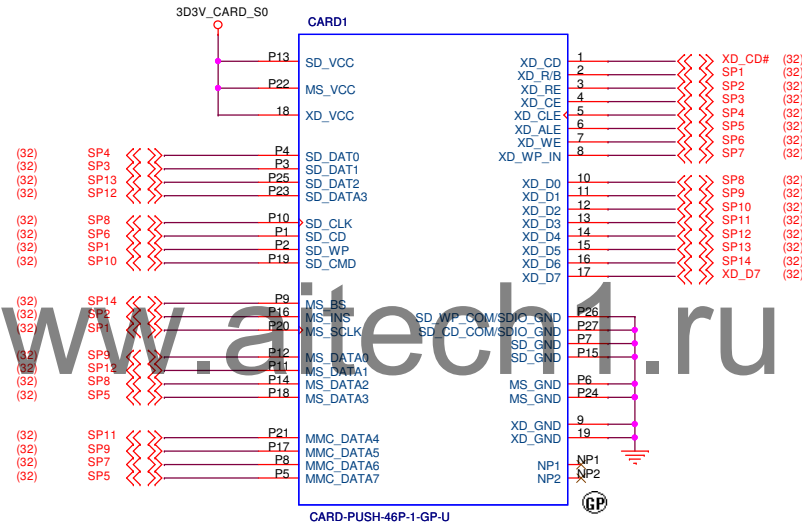
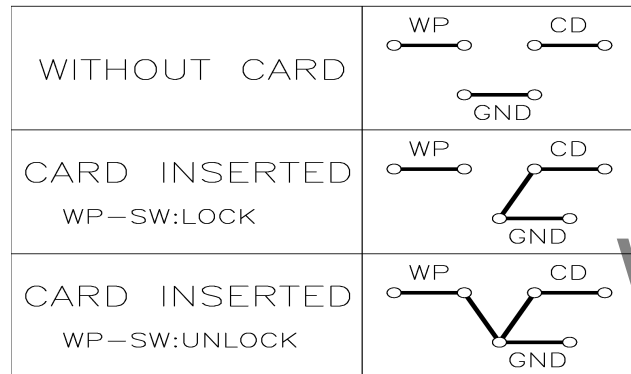
Size A3	Document Number Nirvana 13	Rev A00
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SSID = SDIO



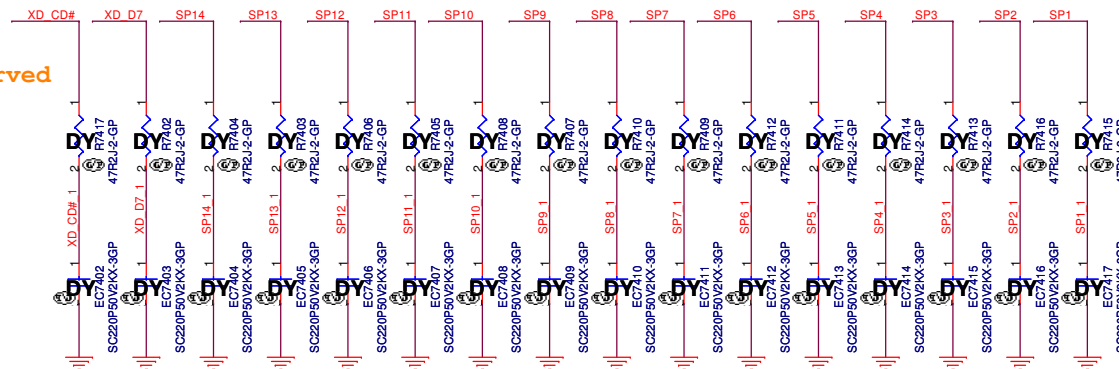
SD/XD/MS/MMC+ Card Reader



20.I0129.001

2nd = 20.I0135.001

For EMI Reserved



PIN	TYPE	FUNCTION	RTSS138 NET
1	SD	SD-DAT2	SP13
2	SD	SD-CD/DAT3	SP12
3	MMC_PLUS	MMC-DAT4	SP11
4	SD	SD-CMD	SP10
5	MMC_PLUS	MMC-DAT5	SP9
6	SD	SD-VSS	POWER
7	SD	SD-VDD	POWER
8	MemoryStick	MS-VSS	POWER
9	MemoryStick	MS-VCC	POWER
10	MemoryStick	MS-SCLK	SP1
11	MemoryStick	MS-DAT3	SP5
12	MemoryStick	MS-INS	SP2
13	MemoryStick	MS-DAT2	SP8
14	MemoryStick	MS-DAT0	SP9
15	MemoryStick	MS-DAT1	SP12
16	MemoryStick	MS-BS	SP14
17	MemoryStick	MS-VSS	POWER
18	SD	SD-CLK	SP8
19	MMC_PLUS	MMC-DAT6	SP7
20	SD	SD-VSS	POWER
21	MMC_PLUS	MMC-DAT7	SP5
22	SD	SD-DAT0	SP4
23	SD	SD-DAT1	SP3
24	SD	SD-COM(SW)	SP1
25	SD	SD-CD(SW)	SP6
26	XD	XD-GND	POWER
27	XD	XD-CD	XD_CD#
28	XD	XD-R/B	SP1
29	XD	XD-RE	SP2
30	XD	XD-CE	SP3
31	XD	XD-CLE	SP4
32	XD	XD-ALE	SP5
33	XD	XD-WE	SP6
34	XD	XD-WP	SP7
35	XD	XD-GND	POWER
36	XD	XD-D0	SP8
37	XD	XD-D1	SP9
38	XD	XD-D2	SP10
39	XD	XD-D3	SP11
40	XD	XD-D4	SP12
41	XD	XD-D5	SP13
42	XD	XD-D6	SP14
43	XD	XD-D7	XD-D7
44	XD	XD-VCC	POWER
45	SD	SD-WP(SW)	SP1

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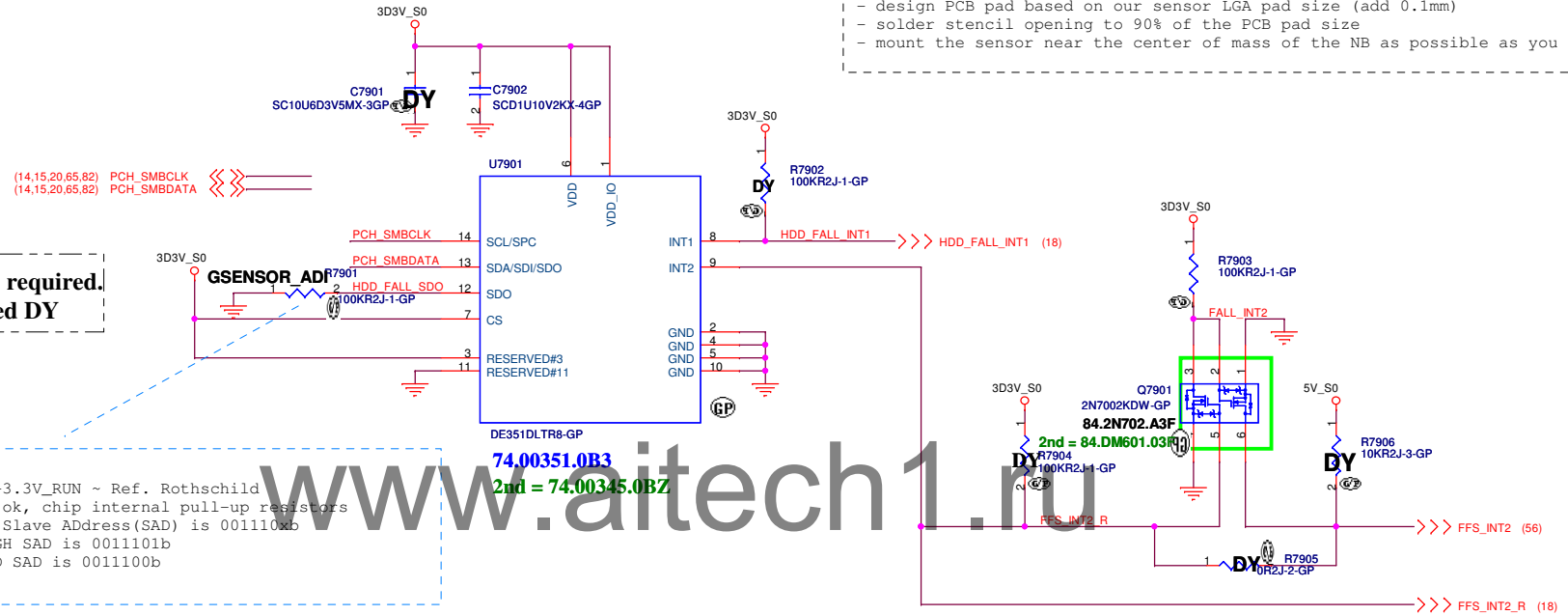
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Free Fall Sensor

| Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



For ADI G-sensor : R7901 is required.
For ST G-sensor : R7901 need DY

09/0422

- (#1) Just pull +3.3V_RUN ~ Ref. Rothschild
- (#2) FAE/ DY is ok, chip internal pull-up resistors
- (#3) From spec, Slave Address(SAD) is 001110xb
 - Pull HIGH SAD is 0011101b
 - Pull GND SAD is 0011100b


Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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IO Board CONN 80 pin

USB3.0 CLK
WWAN USB

WWAN PCIE
WWAN PCIE

WWAN SMBUS

LAN PCIE
LAN PCIE

(20) CLK_PCIE_USB3
(20) CLK_PCIE_USB3#
(18) USB_PP4
(18) USB_PN4

(38) PS_ID_R
(20) PCIE_RXP3
(20) PCIE_RXN3
(20) PCIE_TXP3
(20) PCIE_TXN3

(4,15,20,65,79) PCH_SMBDATA
(14,15,20,65,79) PCH_SMBCLK

(20) CLK_PCIE_WWAN_REQ#
(22) 3G_EN
(68) WWAN_LED#
(18) USB30_SMI#

(20) PCIE_RXP2
(20) PCIE_RXN2
(20) PCIE_TXP2
(20) PCIE_TXN2
(20) PCIE_CLK_LAN_REQ#

IOBD1

NP4 80

NP1 1

NP2 40

NP3 40

NP4 80

NP1 1

NP2 40

NP3 40

NP4 80

NP1 1

NP2 40

NP3 40

NP4 80

NP1 1

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NP4 80

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(AC mode)

Within logic high level and disable if it is less than the logic low level.

VIRIF_Sus must be powered up before Vocals1_3, or after Vocals1_3 within 0.7 V. Also, VIRIF_Sus must power down after Vocals1_3, or before Vocals1_3 within 0.7 V.

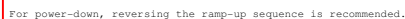
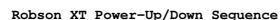
Not floating.

Sense the power button status

This signal has an internal pull-up resistor and has an internal 16 ns de-bounce on the input.

VSRIF must be powered up before Vcc1_3, or after Vcc1_3 within 0.7 V. Also, VSRIF must power down after Vcc1_3, or before Vcc1_3 within 0.7 V.

This signal represents the Power Good for all the non-CORE and non-machine power rails.



red word: KBC GPIO

Sense the power button status

VSRF_Sns must be powered up before VocSns1_3, or after VocSns1_3 within 0.7 V. Also, VSRF_Sns must power down after VocSns1_3, or before VocSns1_3 within 0.7 V.

VSRIF must be powered up before Vcc1_3, or after Vcc1_3 within 0.7 V. Also, VSRIF must power down after Vcc1_3, or before Vcc1_3 within 0.7 V.


This signal represents the Po
Good for all the non-COPE and
non-musshing young balls

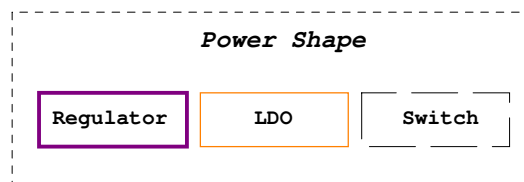
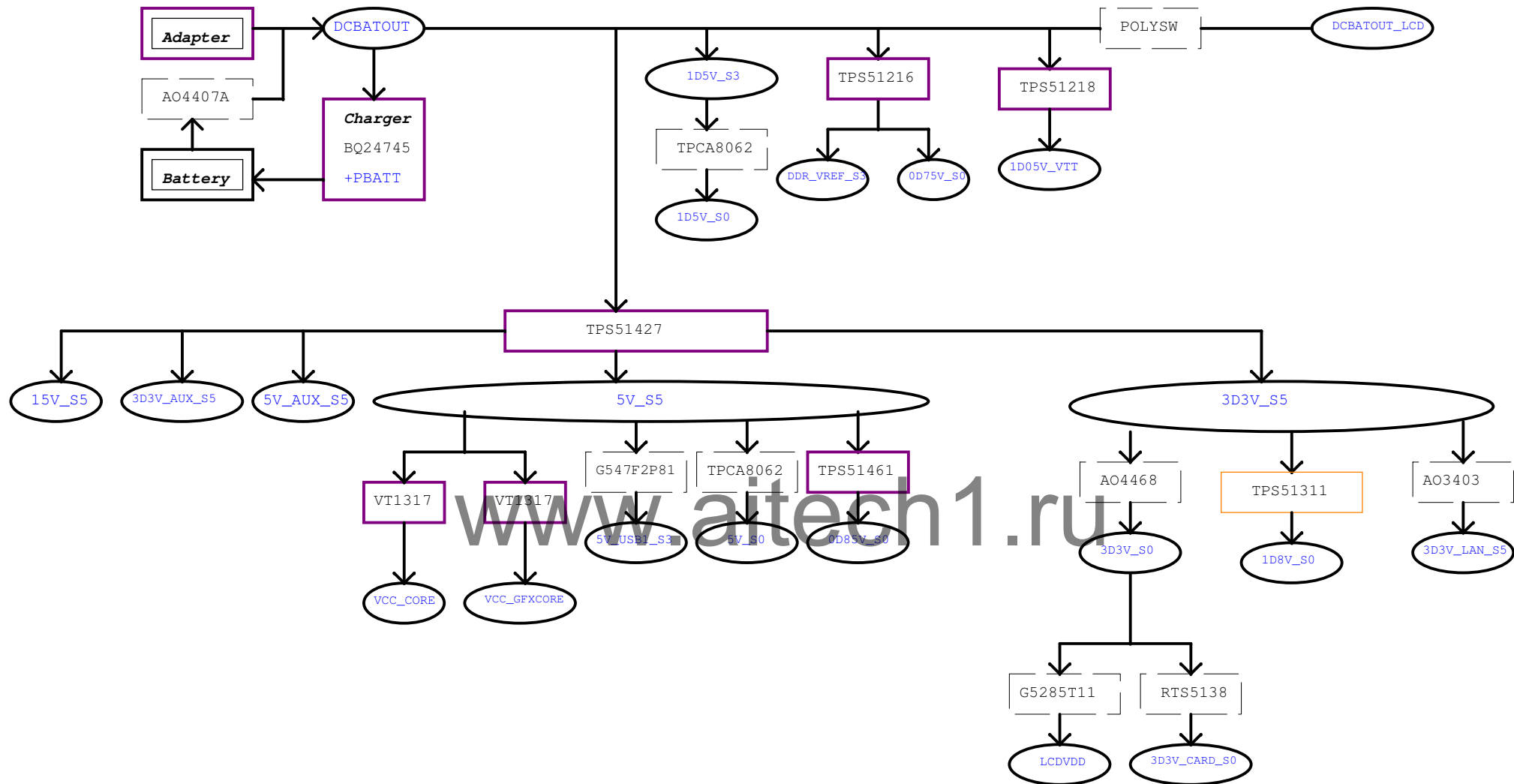


The diagram illustrates the power management architecture for the W6505G. Key components and their connections include:

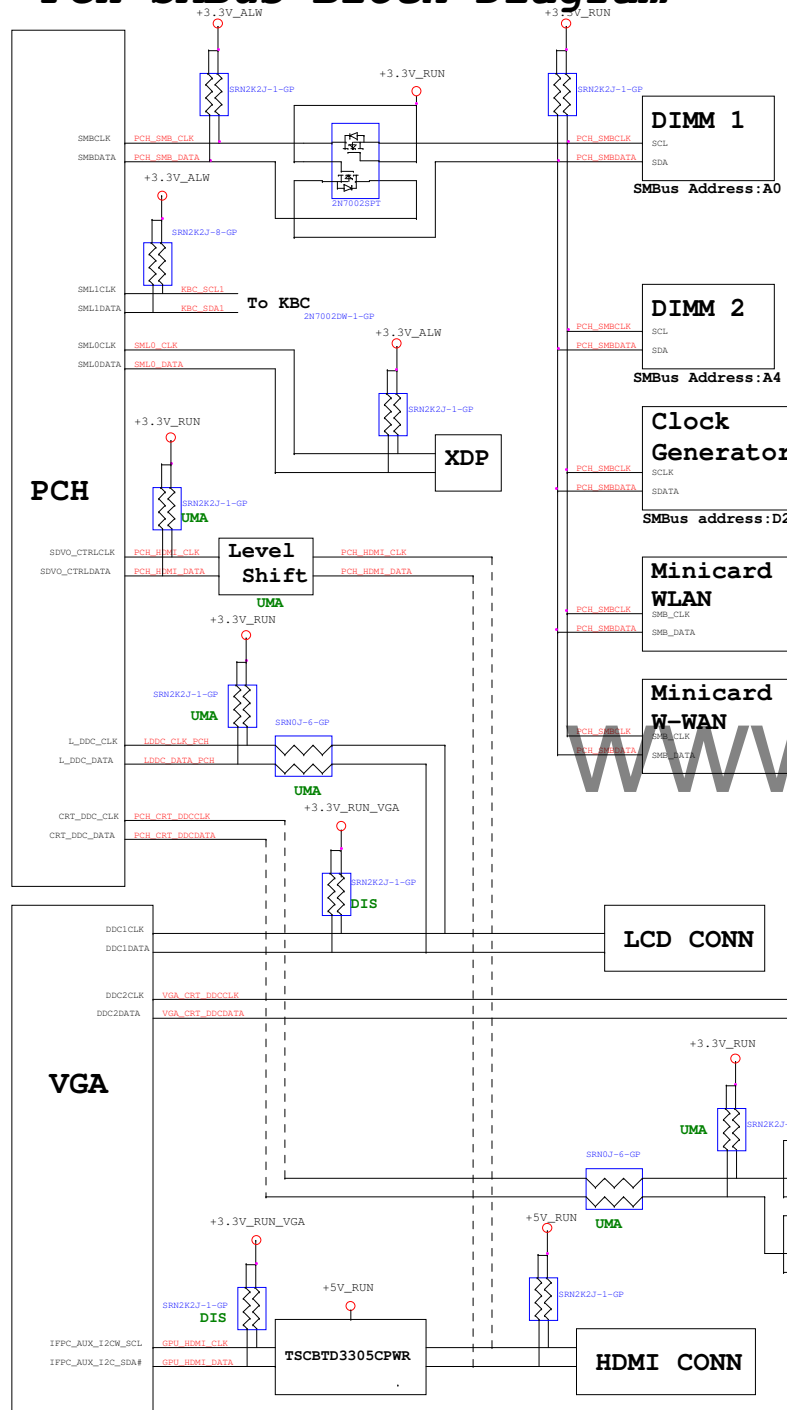
- Power Sources:** AC Adapter in (Page 39), DC Battery (Page 39), and BT+ BQ24745 Charger (Page 40).
- Regulators:**
 - TPS51116RGER:** 1D5V_S3, DDR_VREF_S3, 0D75V_S0, RUNPWROK.
 - TPS53311RGRTR:** 1D8V_S0, RUNPWROK.
 - TPS51218DSCR:** 1D05_VTT, 1.05VTT_PWRGD.
 - RT8208BGQW:** 0D85_S0, D85V_PWRGD.
 - ISL95831HRTZ:** VCC_CORE, VCC_GFXCORE, IMVP_PWRGD.
- Control Logic:**
 - KBC NPCE795P:** GPIOs for PM_SLP_S4#, PM_SLP_S3#, PM_SLP_S4#, PM_SLP_S3#, PM_SLP_S4#, PM_SLP_S3#.
 - Cougar Point PCH:** SLP_S4#, SLP_S3#, DRAMPWRGD, PROC_PWRGD, PLTRST#, PWRBTN#, RSMRST#, PM_PWRBTN#, S0_PWR_GOOD, APWRGD, PWRGD, SYS_PWRGD, SYS_PWRGD.
 - Sandy Bridge CPU:** SM_DRAMPWRGD, UNICORE_PWRGD, RSTIN#, SVID, SVID.
- Other Components:**
 - RT8223MGQW DC/DC (3V/5V):** 5V_S5, 3D3V_S5, 15V_S5, 3V_AUX_S5, 3D3V_AUX_S5, 3V_S5_POK, S5_ENABLE.
 - TPS51218DSCR:** 1D05_VTT, 1.05VTT_PWRGD.
 - RT8208BGQW:** 0D85_S0, D85V_PWRGD.
 - ISL95831HRTZ:** VCC_CORE, VCC_GFXCORE, IMVP_PWRGD.

The diagram also includes a large watermark "www.aitech1.ru" and a "Core Design" logo for Wistron Corporation.

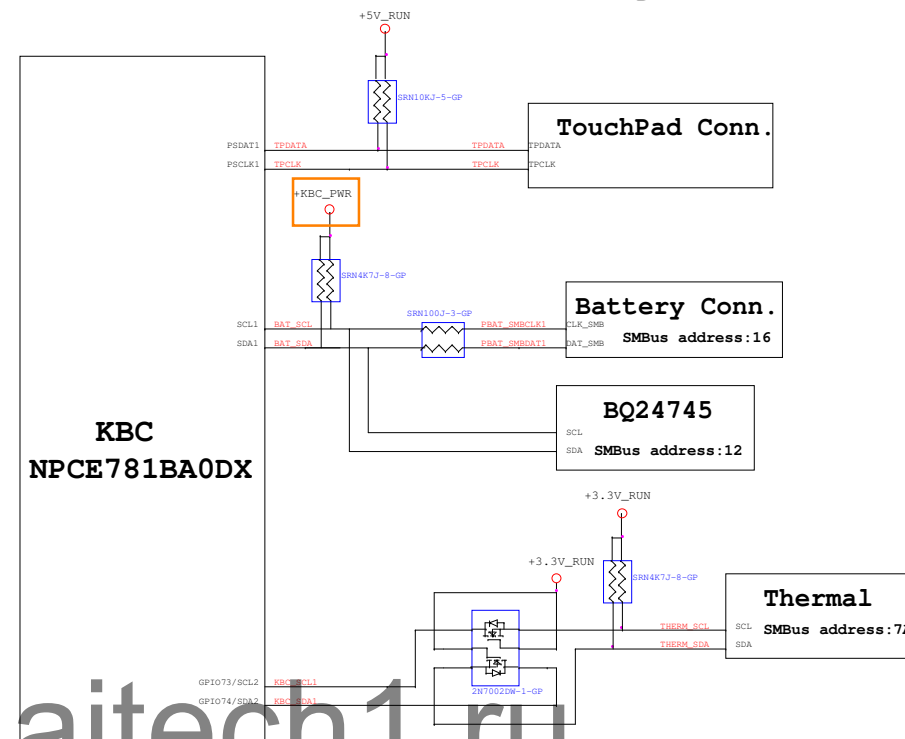
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Power Up Sequence Diagram	
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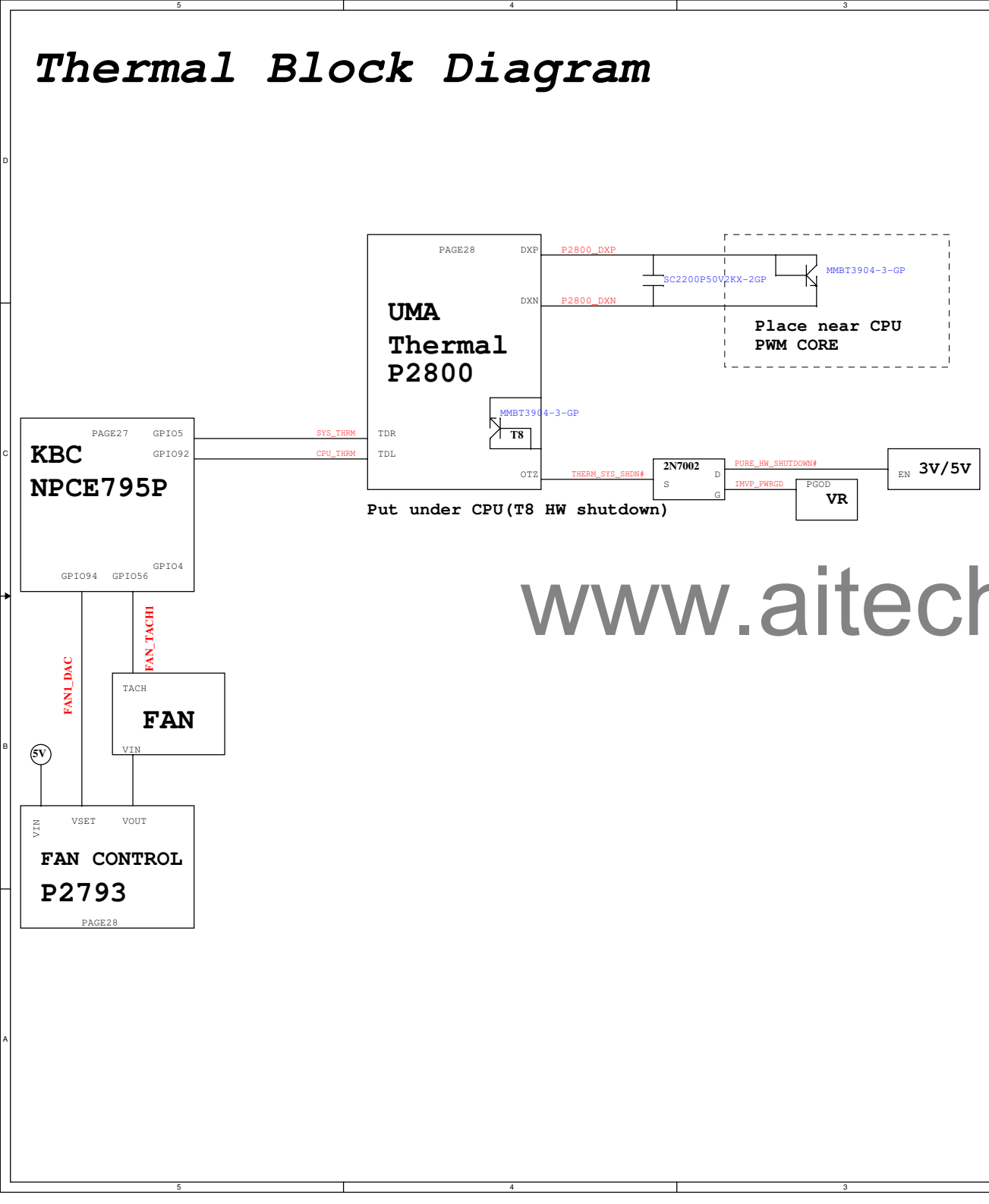


PCH SMBus Block Diagram



KBC SMBus Block Diagram



[illegible]

Audio Block Diagram

The diagram illustrates the audio block architecture. On the left is the **Codec 92HD79B1**. It has several output and input pins:

- SPKR_PORT_D_L-** and **SPKR_PORT_D_L+** are connected to the **SPEAKER** block.
- HP1_PORT_B_L** and **HP1_PORT_B_R** are connected to the **HP OUT** block.
- HP0_PORT_A_L**, **HP0_PORT_A_R**, and **VREFOUT_A_OR_F** are connected to the **MIC IN** block.
- DMIC_CLK/GPIO1** and **DMIC0/GPIO2** are connected to the **Digital MIC** block.
- PORTC_L**, **PORTC_R**, and **VREFOUT_C** are connected to the **Analog MIC** block.

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Thermal/Audio Block Diagram

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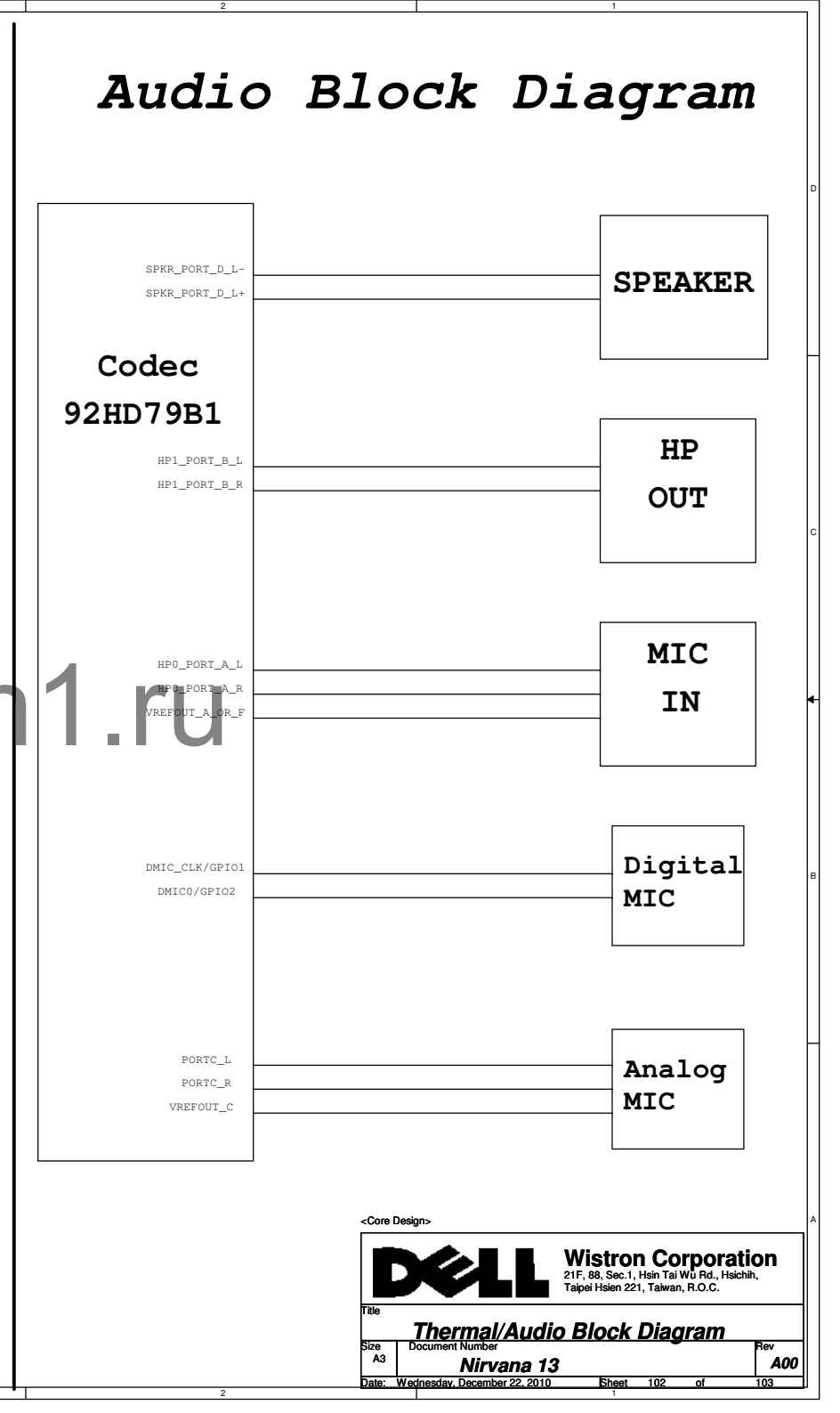
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Version	Date	Page	Function	Change Item
A00	20101222	40	Power	Power/Brian: Change PR4047 to 174k ohm from 121k ohm. Change PR4035 to 300k from 49.9k. Change PR4031 to 150k from 0 ohm. Change PR4034 to 0 ohm pad. Stuff PQ4003. Change PR4036 to 0 ohm pad. Stuff PQ4004. Change PR4037 to 76.8k ohm from 49.9k ohm. Change PR4032 to 0 ohm pad.
A00	20101222	42	Power	Power/Brian: Change PU4201 to 74.01316.F33.
A00	20101224		EE	Change all of 0ohm to short pad at X-build stage: 0402: R1404 R1405 R1503 R1504 R5010-R5012 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R3614 R3710 0603: R5803 R5804 R8507 Parallel resistor: RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2016 RN5117,RN5112,RN5113,RN5114,RN5115
A00	20101224		EE	Rename PRN3901 to PN3901. Rename PTC4101-PTC4103 to PT4101-PT4103. Rename PTC4502,PTC4509 to PT4502-PT4509. Rename PTC4601,PTC4602 to PT601-PT4602. Rename PTC4801 to PT4801. Rename LINEOUT1 to LOUT1. Rename PWRBTN1 to PWRBT1. Rename HALLSW1 to LID1.
A00	20101224	27	EE	Change R2724 to 47K from 33K.
A00	20101224	28	EE	If stuff P2800EA1 then must stuff R2803,R2804 C2805 but if stuff P28003B0 should be un-stuff.
A00	20101224	45,46	Power	Change PR4514,PR4607 to 0ohm short pad from 0402 and un-stuff PC4523 at X-Build stage.
A00	20101224	28	EE	If stuff P2800EA1 then must stuff R2803,R2804 C2805 but if stuff P28003B0 should be un-stuff.
A00	20101227	32,42,49 62,64,65 69,70	EE	Change R3210,R3211:PR4217-PR4220,PR4254;R4908,R4909,R4903,R4910,R4913-R4916, R4917,R4918;R6205;R6403,R6404;R6511;R6902;R7002 to 0R 0402 pad.
A00	20101228	23	EE	0402 0R pad: R2301.
A00	20101228	27,62,82	EE	VGA_THRM change to USB_PWR_EN.
A00	20101228	27	EE	Change R2756,R2763,R2766 to 0R short pad.
A00	20101228	28	EE	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at X-Build.
A00	20101229	71	EE	DB1 change to ZZ.00PAD.Y41(solder mask type) and keep un-stuff at X-Build stage.
A00	20101229	27,62,82	EE	Rename USB_PWR_EN to USB3_PWR_ON. Remove R6205,R620. Remove R2809 and R8210. Connect USB3_PWR_ON from KBC to IOBD1.61.
A00	20101230	41,46,65	EE	Change PR4119 to 0R short pad. Change PR4114 to 0R short pad. Follow the standard schematics: remove PR4615,PR4616. Change R6406,R6405 to 0R short pad. Change PR4116 to 0R0603 short pad. Change PR4106 to 0R0603 short pad. Change R6510 to 0R 0603 pad. Change PR4103,PR4104 to 0R0805 short pad.
A00	20101231	43	Power	Power/Brian: change PL4201 to 68.2415N.101 from 68.10110.10G.
A00	20101231	42,50,18 14,9,8	EE	Change PR4209,PR4212 to PN4201 10k array resistor. Change R5004,R5005 to RN5001 33 ohm array resistor. Merge R1804,R1806 to RN1804 22 ohm array resistor. Merge R1401,R1402 to RN1401 10k ohm array resistor. Merge R906,R907 to RN902 100 ohm array resistor. Merge R801,R802 to RN801 100 ohm array resistor.
A00	20110103	68,82	EE	Change R6801,R8201-R8203 to 1k.
A00	20110103	68,82	EE	Change R6801,R8201-R8203 to 1k.
A00	20110104	5	EE	merge R512,R514 to RN502 1k array resistor.
A00	20110104	8	EE	Swap VCC_CORE to RN801.4 and VCCSENSE to RN801.1.
A00	20110104	9	EE	Swap VCC_GFXCORE to RN902.1 and VCC_AXG_SENSE to RN902.4.
A00	20110104	14	EE	Change RN1401 to 0R short pad.
A00	20110104	15	EE	Change R1502 to 0R0402 short pad.
A00	20110104	17	EE	Merge RN1701,RN1706 to RN1703 2.2k array resistor.
A00	20110104	32,49,57 64	EE	Remove TR3201,TR4902,R5718,R5719,TR6401
A00	20110104	68,69	EE	Change R6804,R6806,R6808,R6810,R6906 to 620 ohm 5%.
A00	20110104	82	EE	Merge R8201-R8203 to RN8201 1k array resistor.
A00	20110107	68,69	EE	Change R6804,R6806,R6808,R6810,R6906 to 1k ohm 5%.

<Core Design>

File

Size

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Version	Date	Page	Function	Change Item
A00	20110107	49	EE	Change F4902 to 0603 0 ohm.
A00	20110110	21	EE	Merge R2115,R2116 to RN2101.
A00	20110110	41	Power	Change PG4110,PG4112,PG4114~PG4119,PG4122,PG4126,PG4129,PG4131,PG4133,PG4135~PG4138,PG4140,PG4142,PG4102~PG4109,PG4111,PG4113,PG4118,PG4120,PG4123,PG4101,PG4127,PG4130,PG4132,PG4134, PG4139,PG4141 to ZZ.CLOSE.001.
A00	20110110	41	Power	Add PT4104 47uF.
A00	20110111	49,51	EE	Change R4908,R4909,R4903,R4910,R4913~R4916 R4917,R4918 to 0R 0402 reisstors. Change R5101~R5108 to 0 ohm array resistors RN5102~RN5105. Change RN5117 to 0 ohm resistor.
A00	20110112	20	EE	Change C2007,C2008 to 15pF from 12pF base on vendor's report.
A00	20110112	41	EE	Change PT4104 to 100uF.
A00	20110113	8,9	EE	Change RN801,RN902 to 100 ohm 1% (66.10156.04L).
A00	20110113	5,8,9 17,18,21 42,82	EE	Swap RN502,RN801,RN902,RN1703,RN1804,RN2101,RN4201,RN8201 base on swap report.
A00	20110118	51	EE	Remove RN5117 for PCH_HDMI_CLK and PCH_HDMI_DATA.
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